WHITE PAPER

FPGA

# Leveraging the Intel® HyperFlex™ FPGA Architecture in Intel Stratix® 10 Devices to Achieve Maximum Power Reduction

## Intel Stratix 10 devices leverage the innovative Intel HyperFlex FPGA architecture to achieve power savings not possible with other FPGAs and SoCs.


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## Introduction

Intel® Stratix® 10 FPGAs and SoCs offer advanced, exclusive features and capabilities for power reduction including SmartVID, hard intellectual property (IP) blocks for commonly used functions and floating-point digital signal processing (DSP), power gating of unused blocks, low-power transceivers, extra low-voltage devices, and extra low-static power devices. Additionally, Intel Stratix 10 devices are the only high-performance FPGAs and programmable SoCs developed on Intel's industry leading 14 nm Tri-Gate process, offering the lowest power in the industry. These device-level and process-level innovations play an important role in power reduction for Intel Stratix 10 devices and are described in other documents such as Meeting the Performance and Power Imperative of the Zettabyte Era. This white paper highlights an additional power reduction advantage available to Intel Stratix 10 users that is unique to the programmable logic industry, leveraging the revolutionary Intel HyperFlex™ FPGA Architecture that enables 2X performance compared to prior programmable logic architectures.

Combined with the advantages of Intel's 14 nm Tri-Gate process, the Intel Stratix 10 Intel HyperFlex FPGA Architecture enables designers to achieve core performance up to 1 GHz. With these performance levels, system designers can opt to reduce the core resources required by their design by increasing their clock frequency and reducing the data path width. The resulting design retains the same throughput as the original implementation, but utilizes fewer device resources. In the simplest case, designers using this technique can double their clock frequency and halve the width of data paths in their designs, while retaining the original overall throughput (see Figure 1).

The reduction in device resources contributes to lower power in two important ways. First, fewer device resources results in less static power consumed by the design, and in many cases, a user can use a smaller device than originally planned. Second, the reduction in devices resources offsets the increase in dynamic power that results from running the design at a higher frequency. This principle can be understood by applying the following equation for dynamic power:

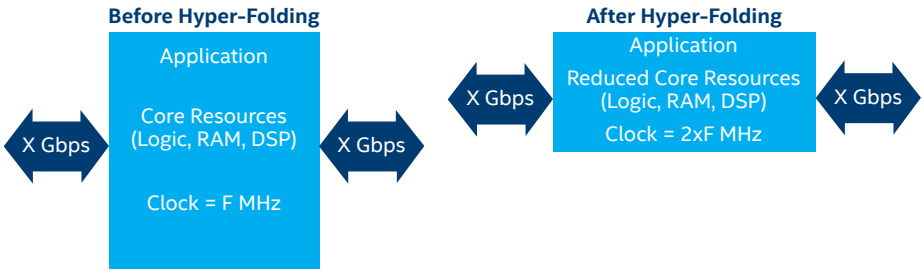


**Figure 1.** Hyper-Folding a Design to Reduce Resource Utilization and Power

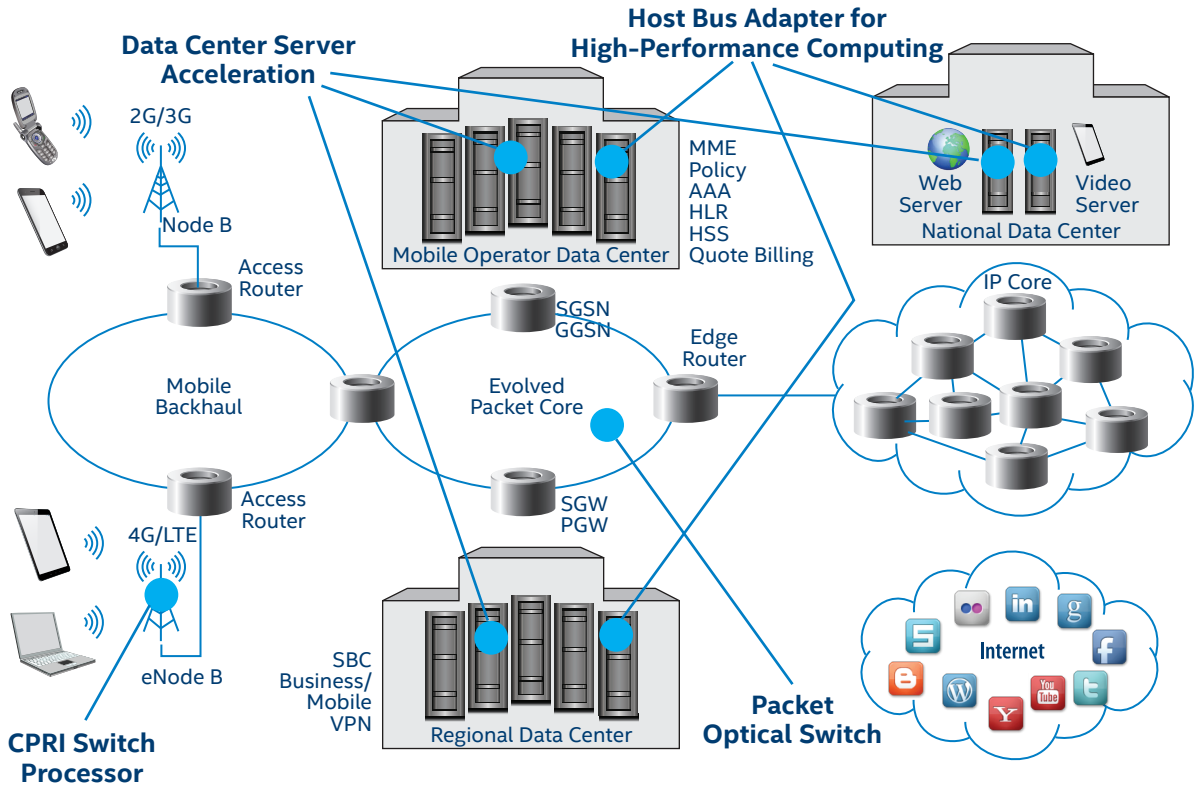


**Figure 2.** High-Performance Applications Throughout the ICT Infrastructure That Benefit from Power Reduction

PowerDynamic = ½ $CV^2F$

The reduction in dynamic power from using fewer logic resources results in a reduction of the capacitance C, which offsets the increase in power from the higher F (frequency). As a result, the most dramatic power reductions possible with Intel Stratix 10 devices—up to 70% decreases in total power—are achieved through leveraging this technique of reducing device resources while increasing the clock frequency, called Hyper-Folding. This paper analyzes and explores the power reductions resulting from Hyper-Folding by presenting four application examples taken from existing high-performance FPGA designs currently being implemented in the communications and data center industries. These four designs are spread throughout the Information and Communications Technology (ICT) infrastructure, and are shown in Figure 2.

## Power reduction in wireline communications: packet optical switch example

The first example is a wireline communications design: a two-stage MUX for a packet optical switch that aggregates multiple 10G links and formats and multiplexes them for processing by a switch fabric. The original design consists of a single Stratix V GX BB device that includes 10 channels of 11.181 Gbps transceiver links, 10 channels of 12.5 Gbps transceiver links, a single PCIe Gen1 x4 link to the main processor, almost 90% utilization of the embedded memory, and 60% utilization of the logic with a main clock of 350 MHz. At 100° C and worst-case operating conditions, this design consumes 47 watts. Figure 3 shows a block diagram of this design.

After applying Hyper-Folding, this design can fit into the Intel Stratix 10 GX 650, which offers about 30% fewer logic

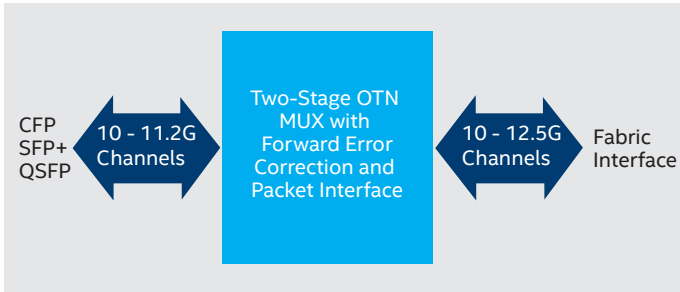


**Figure 3.** Two-Stage MUX for Packet Optical Switch

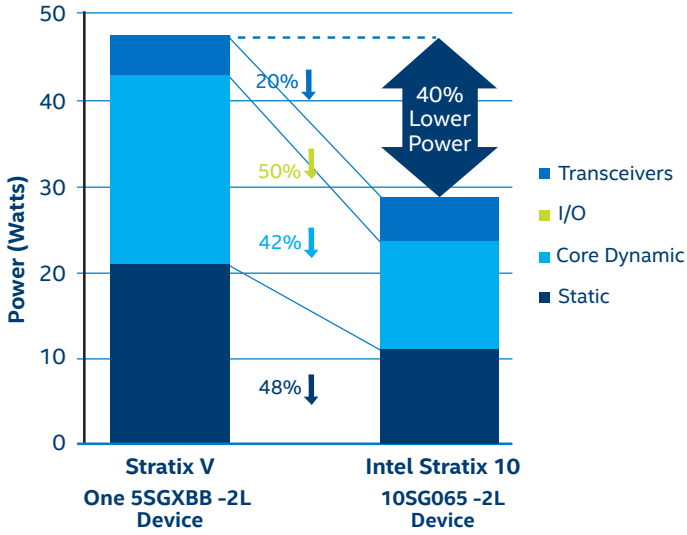


**Figure 4.** Intel Stratix 10 Power Reduction of a Wireline Optical Switch Application

element resources than the Stratix V GX BB device. Operating at 700 MHz (2 x 350 MHz), the design consumes less than 29 watts, which represents a 40% reduction in total power from the original implementation. Figure 4 shows the total power reduction of this design and a breakdown of the reduction of each of the component power elements when Hyper-Folding is leveraged to its maximum extent to reduce power.

## Power reduction in wireless communications: CPRI switch processor example

The second example is a wireless infrastructure design that processes and switches multiple low-latency data streams for mobile communication. The design, called a 24x24 CPRI switch processor, occupies a single Stratix V GX AB device, with over 80% logic utilization and 48 channels of 10 Gbps data streams (24 in and 24 out), and includes a main clock that runs at 245 MHz. At 100° C and under worst-case operating conditions, the power consumption of the Stratix V version of this design is 48 watts. Figure 5 shows a block diagram on this design.

After applying Hyper-Folding, this design can fit into the Intel Stratix 10 GX 1100 device and run at 491 MHz. The Intel Stratix 10 design consumes 25.3 watts, which represents a nearly 50% reduction in total power from the prior implementation. Figure 6 shows the total power reduction of this design, when Hyper-Folding is applied to it. See Figure 6.

## Power reduction in high-performance computing: host bus adapter example

The third example is a host bus adapter for high-performance computing design that aggregates several non-volatile memory express (NVME) interfaces. The base design consists of two Stratix V GX A5 devices that include three NVME interfaces and one PCIe Gen3 x16 interface each, as well as a RAID engine and blocks for compression and 256-bit AES encryption. Each Stratix V device is 80% utilized in terms of logic elements, and over 75% utilized in terms of embedded M20K memory blocks. The design also makes use of partial reconfiguration to implement different compression algorithms while in operation. Operating at 245 MHz, this design consumes 61.5 watts. Figure 7 shows a block diagram of this design.

When HyperFolded, this enterprise storage controller design fits into a single Intel Stratix 10 GX 1100 device. Operating at 490 MHz, the design consumes less than 23 watts, which represents a 63% reduction in total power from the prior implementation. Figure 8 shows the total power reduction of this design when implemented in a Intel Stratix 10 device compared to the prior generation implementation.

## Power reduction in the data center: server acceleration example

The final application is a high-performance computing accelerator for data centers. The design involves FPGAs communicating with the main processors in the server blades via PCI Express* (PCIe*) and interacting with Ethernet streams through multiple 10 Gbps transceiver channels. In a Stratix V-based implementation, the base design occupies five Stratix V GS D5 devices, each with eight 10 Gbps transceiver channels and a single PCIe Gen2 x8 interface. The design uses Stratix V GS D5 devices because they offer

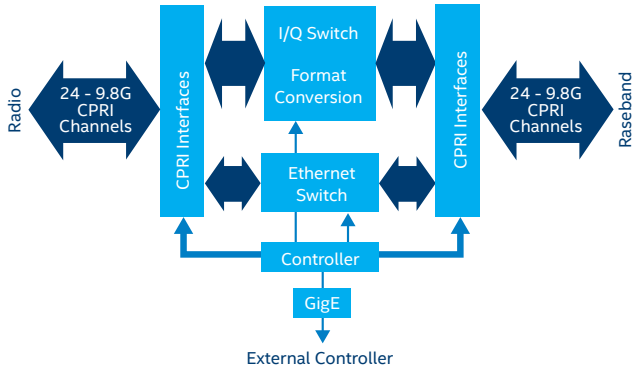


**Figure 5.** Wireless Infrastructure Design (24x24 CPRI Processor Switch)

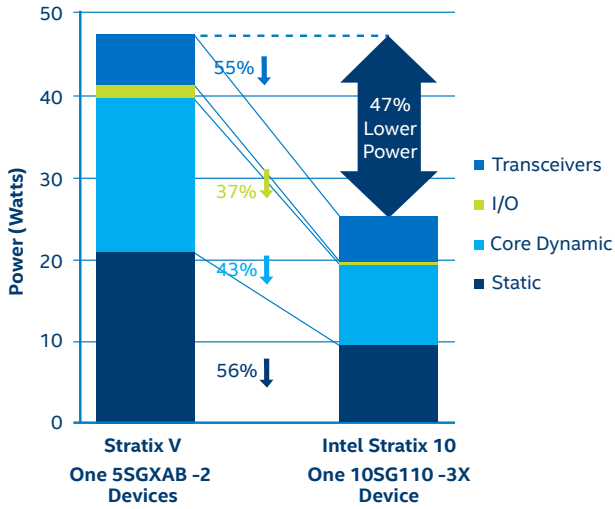


**Figure 6.** Intel Stratix 10 Power Reduction of a Wireless Infrastructure Application

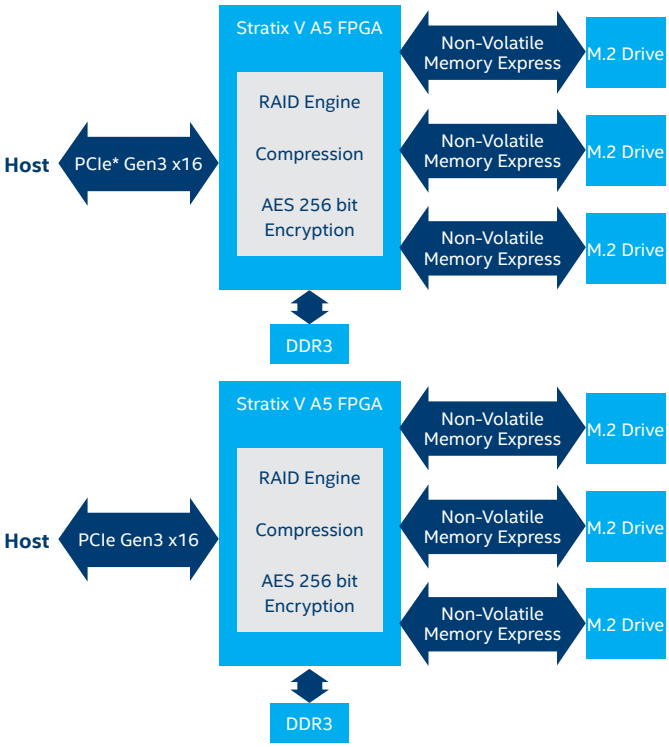


**Figure 7.** Host Bus Adapter for HIgh-Performance Computing

a high multiplier count to support the high-performance DSP operations often found in algorithm acceleration applications, and partial reconfiguration is also leveraged to dynamically update the acceleration algorithms in system as needed. Each Stratix V device also features a DDR3x72 interface operating at 800 MHz, and the main clock in the design is operating at 250 MHz. Figure 9 shows a block diagram of this design.

When implemented in Stratix V devices, and operating at the highest allowed junction temperature of 100° C, the five devices together consume 150 watts in the worst case. In the Intel Stratix 10 version, the DDR3 memory interfaces are replaced by two DDR4 x144 memory interfaces running at 1333 Mbps. When implemented with Hyper-Folding and operating at 500 MHz, this design fits into a single Intel Stratix 10 GX 2100 device and consumes less than 45 watts, resulting in a total power reduction of 70%. A large portion of these savings are due to the effectiveness of Hyper-Folding, but other contributors include:

- Lower dynamic power due to:
  - Lower device capacitance resulting from the advanced 14 nm Tri-Gate process
  - SmartVID reduction of the operating voltage to the lowest possible level

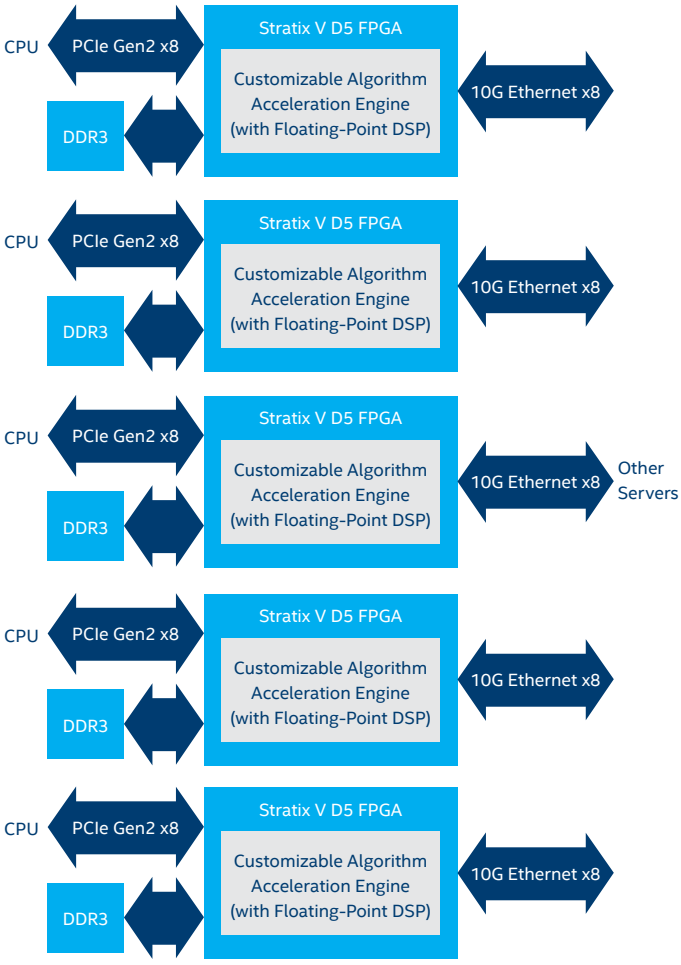


**Figure 9.** Data Center Server Acceleration Application

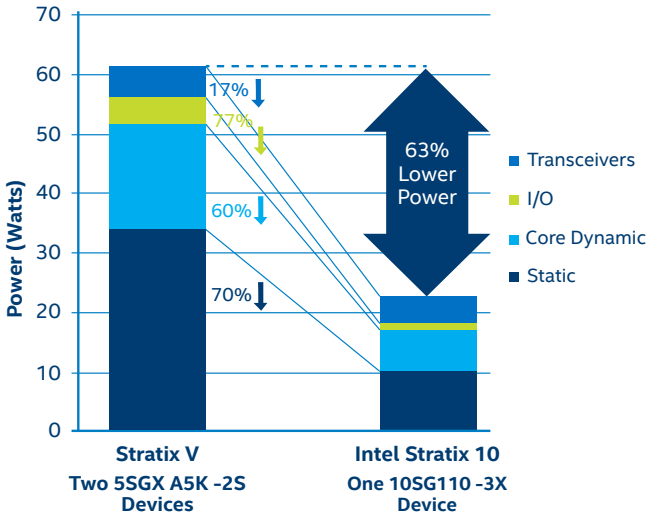


**Figure 8.** Intel Stratix 10 Power Reduction of an Enterprise Storage ControllerComputing

- Hard memory controllers that reduce FPGA resource utilization while delivering the highest interface performance in the industry
- Hard IP blocks for floating-point DSP operations that reduce FPGA resource utilization while delivering the highest performance for algorithm acceleration
- Lower I/O power due to consolidation of the memory interfaces into fewer, higher performance interfaces
- Lowest transceiver power in high-end FPGAs and programmable SoCs

Figure 10 shows the total power reduction realized by Hyper-Folding this design, and includes a breakdown of the reductions across the various device categories of core dynamic power, static power, I/O power, and transceiver power.

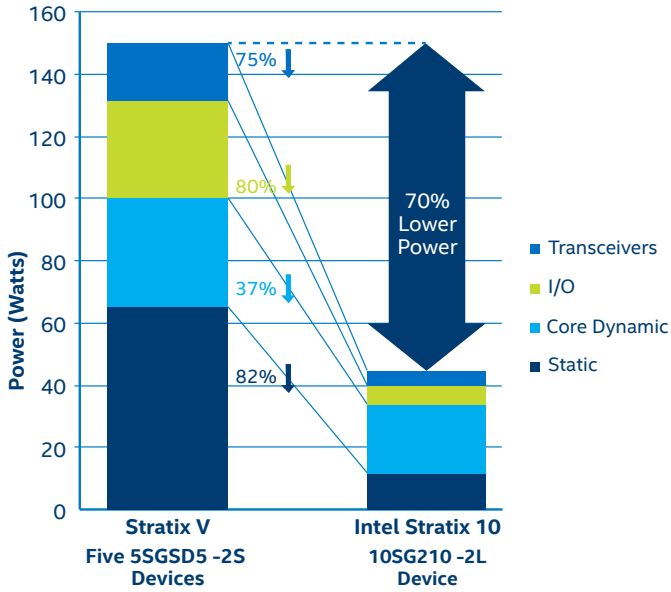


**Figure 10.** Stratix 10 Power Reduction of a Data Center Server Acceleration ApplicationComputing

## Conclusion

Intel Stratix 10 devices offer today's designers the most advanced power reduction techniques available in high-performance FPGAs and SoCs. In addition to a broad range of device-level features and Intel's low-power 14 nm FinFET process, Intel Stratix 10 devices also offer the unique capability to leverage the innovative Intel HyperFlex FPGA Architecture to Hyperfold designs and achieve power savings not possible with other FPGAs and SoCs. The effectiveness of Hyper-Folding on total power is illustrated with four high-performance applications, and the results are summarized in Table 1.

| Application | Stratix V Device(s) | Power Consumption | Intel Stratix 10 Device (HyperFolded) | Power Consumption | Power Reduction |
|---|---|---|---|---|---|
| Two-Stage Multiplexer for Packet Optical Switch | 1 x GX BB | 47 W | 1x GX 650 | 28.4 W | 40% |
| 24x24 CPRI Switch Processor | 1 x GX AB | 48 W | 1 x GX 1100 | 25.3 W | 47% |
| Host Bus Adapter for High-Performance Computing | 2 x GX A5 | 61.5 W | 1x GX 1100 | 23 W | 63% |
| Data Center Server Accelerator | 5 x GS D5 | 150 W | 1 x GX 2100 | 44.8 W | 70% |

**Table 1.** Summary of Total Power Reduction Across High-Performance Application Examples with Intel Stratix 10 Devices

Leveraging the many power reduction techniques available in Intel Stratix 10 devices, including Hyper-Folding, power reductions of up to 70% compared to prior high-performance FPGA implementations are possible, enabling designers to achieve the lowest power for today's high-performance applications.

## Where to Get More Information

For more information about Intel and Intel Stratix 10 FPGAs, visit **https://www.altera.com/products/fpga/stratix-series/stratix-10/overview.html**

[1] http://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/wp/wp-01200-power-performance-zettabyte-generation-10.pdf
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