Intel® Xeon® Processor
C5500/C3500 Series and LGA1366 Socket

Thermal/Mechanical Design Guide

August 2010
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# Revision History

<table>
<thead>
<tr>
<th>Revision Number</th>
<th>Description</th>
<th>Revision Date</th>
</tr>
</thead>
</table>
| 002             | Modified Table 5-3, Socket and ILM Mechanical Specifications  
|                 | Modified Section 7.6.1, Fan Speed Control     | August 2010     |
| 001             | First release                                 | February 2010   |
Introduction

This document provides guidelines for the design of thermal and mechanical solutions for processors in the Picket Post platform. The components described in this document include:

- The processor thermal solution (heatsink) and associated retention hardware.
- The LGA1366 socket and the Independent Loading Mechanism (ILM) and back plate.

The goals of this document are:

- To assist board and system thermal mechanical designers.
- To assist designers and suppliers of processor heatsinks.

Other processor specifications are provided in the Intel® Xeon® Processor C5500/C3500 Series Datasheet.
1.1 Reference Documents

Material and concepts in the following documents may be beneficial when reading this document.

Table 1-1. Reference Documents

<table>
<thead>
<tr>
<th>Document</th>
<th>Document#</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>European Blue Angel Recycling Standards</td>
<td></td>
<td>3</td>
</tr>
<tr>
<td>Intel® Xeon® Processor C5500/C3500 Series Datasheet, Volume 1</td>
<td>323103</td>
<td>1</td>
</tr>
<tr>
<td>Intel® Xeon® Processor C5500/C3500 Series Datasheet, Volume 2</td>
<td>323317</td>
<td>1</td>
</tr>
<tr>
<td>Intel® Xeon® Processor 5500 Series Mechanical Model</td>
<td>321326</td>
<td>2</td>
</tr>
<tr>
<td>Intel® Xeon® Processor 5500 Series Thermal Model</td>
<td>321327</td>
<td>2</td>
</tr>
<tr>
<td>Entry-level Electronics Bay Specification</td>
<td></td>
<td>4</td>
</tr>
</tbody>
</table>

Notes:
1. See http://developer.intel.com/design/intarch/xeon5000/documentation.htm
3. Available at http://www.blauer-engel.de
4. Available at http://ssiforum.oaktree.com/

1.2 Definition of Terms

Table 1-2. Terms and Descriptions (Sheet 1 of 2)

<table>
<thead>
<tr>
<th>Term</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bypass</td>
<td>Bypass is the area between a passive heatsink and any object that can act to form a duct. For this example, it can be expressed as a dimension away from the outside dimension of the fins to the nearest surface.</td>
</tr>
<tr>
<td>DTS</td>
<td>Digital Thermal Sensor reports a relative die temperature as an offset from TCC activation temperature.</td>
</tr>
<tr>
<td>FSC</td>
<td>Fan Speed Control</td>
</tr>
<tr>
<td>IHS</td>
<td>Integrated Heat Spreader: a component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.</td>
</tr>
<tr>
<td>ILM</td>
<td>Independent Loading Mechanism provides the force needed to seat the 1366-LGA land package onto the socket contacts.</td>
</tr>
<tr>
<td>IMON</td>
<td>The current monitor input to the CPU. The VRM tells the CPU how much current it is drawing.</td>
</tr>
<tr>
<td>LGA1366 socket</td>
<td>The processor mates with the system board through this surface mount, 1366-land socket.</td>
</tr>
<tr>
<td>PECI</td>
<td>The Platform Environment Control Interface (PECI) is a one-wire interface that provides a communication channel between Intel processor and chipset components to external monitoring devices.</td>
</tr>
<tr>
<td>$\Psi_{CA}$</td>
<td>Case-to-ambient thermal characterization parameter (psi). A measure of thermal solution performance using total package power. Defined as $\Delta T_{CASE}$ = $T_{LA}$ / Total Package Power. Heat source should always be specified for $\Psi$ measurements.</td>
</tr>
<tr>
<td>$\Psi_{CS}$</td>
<td>Case-to-sink thermal characterization parameter. A measure of thermal interface material performance using total package power. Defined as $\Delta T_{CASE}$ = $T_{S}$ / Total Package Power.</td>
</tr>
<tr>
<td>$\Psi_{SA}$</td>
<td>Sink-to-ambient thermal characterization parameter. A measure of heatsink thermal performance using total package power. Defined as $\Delta T_{SA}$ = $T_{S}$ / Total Package Power.</td>
</tr>
<tr>
<td>$\Delta T_{CASE}$</td>
<td>The case temperature of the processor, measured at the geometric center of the topside of the IHS.</td>
</tr>
<tr>
<td>$\Delta T_{CASE_MAX}$</td>
<td>The maximum case temperature as specified in a component specification.</td>
</tr>
</tbody>
</table>
Introduction

Table 1-2. Terms and Descriptions (Sheet 2 of 2)

<table>
<thead>
<tr>
<th>Term</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCC</td>
<td>Thermal Control Circuit: Thermal monitor uses the TCC to reduce the die temperature by using clock modulation and/or operating frequency and input voltage adjustment when the die temperature is very near its operating limits.</td>
</tr>
<tr>
<td>TCONTROL</td>
<td>Tcontrol is a static value below TCC activation used as a trigger point for fan speed control.</td>
</tr>
<tr>
<td>TDP</td>
<td>Thermal Design Power: Thermal solution must be designed to dissipate this target power level. TDP is not the maximum power that the processor can dissipate.</td>
</tr>
<tr>
<td>Thermal Monitor</td>
<td>A power reduction feature designed to decrease temperature after the processor has reached its maximum operating temperature.</td>
</tr>
<tr>
<td>Thermal Profile</td>
<td>Line that defines case temperature specification of a processor at a given power level.</td>
</tr>
<tr>
<td>TIM</td>
<td>Thermal Interface Material: The thermally conductive compound between the heatsink and the processor case. This material fills the air gaps and voids, and enhances the transfer of the heat from the processor case to the heatsink.</td>
</tr>
<tr>
<td>TLA</td>
<td>The measured ambient temperature locally surrounding the processor. The ambient temperature should be measured just upstream of a passive heatsink or at the fan inlet for an active heatsink.</td>
</tr>
<tr>
<td>TSA</td>
<td>The system ambient air temperature external to a system chassis. This temperature is usually measured at the chassis air inlets.</td>
</tr>
<tr>
<td>U</td>
<td>A unit of measure used to define server rack spacing height. 1U is equal to 1.75 in, 2U equals 3.50 in, etc.</td>
</tr>
</tbody>
</table>
2 Package Mechanical Specifications

2.1 Package Mechanical Specifications

The processor is packaged in a Flip-Chip Land Grid Array (FC-LGA6) package that interfaces with the motherboard via an LGA1366 socket. The package consists of a processor mounted on a substrate land-carrier. An integrated heat spreader (IHS) is attached to the package substrate and core and serves as the mating surface for processor component thermal solutions, such as a heatsink. Figure 2-1 shows a sketch of the processor package components and how they are assembled together. See Section 3 and Section 4.

The package components shown in Figure 2-1 include the following:

- Integrated Heat Spreader (IHS)
- Thermal Interface Material (TIM)
- Processor core (die)
- Package substrate
- Capacitors

Figure 2-1. Processor Package Assembly Sketch

Note:
1. Socket and motherboard are included for reference and are not part of processor package.
2.1.1 Package Mechanical Drawing

The package mechanical drawings are shown in Figure 2-2 and Figure 2-3. The drawings include dimensions necessary to design a thermal solution for the processor. These dimensions include:

1. Package reference with tolerances (total height, length, width, etc.)
2. IHS parallelism and tilt
3. Land dimensions
4. Top-side and back-side component keep-out dimensions
5. Reference datums
6. All drawing dimensions are in mm
2.1.2 Processor Component Keep-Out Zones

The processor may contain components on the substrate that define component keep-out zone requirements. A thermal and mechanical solution design must not intrude into the required keep-out zones. Do not contact the Test Pad Area with conductive material. Decoupling capacitors are typically mounted to either the topside or land-side of the package substrate. See Figure 2-2 and Figure 2-3 for keep-out zones. The location and quantity of package capacitors may change due to manufacturing efficiencies but will remain within the component keep-in.

2.1.3 Package Loading Specifications

Table 2-1 provides load specifications for the processor package. These maximum limits should not be exceeded during heatsink assembly, shipping conditions, or standard use condition. Exceeding these limits during test may result in component failure. The processor substrate should not be used as a mechanical reference or load-bearing surface for thermal solutions.

Table 2-1. Processor Loading Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Maximum</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static Compressive Load</td>
<td>890 N [200 lbf]</td>
<td>1, 2, 3</td>
</tr>
<tr>
<td>Dynamic Compressive Load</td>
<td>1779 N [400 lbf]</td>
<td>1, 2, 3, 4</td>
</tr>
</tbody>
</table>

Notes:
1. These specifications apply to uniform compressive loading in a direction normal to the processor IHS.
2. This is the maximum static force that can be applied by the heatsink and Independent Loading Mechanism (ILM).
3. These specifications are based on limited testing for design characterization. Loading limits are for the package constrained by the limits of the processor socket.
4. Dynamic loading is defined as an 11 ms duration average load superimposed on the static load requirement.

2.1.4 Package Handling Guidelines

Table 2-2 includes a list of guidelines on package handling in terms of recommended maximum loading on the processor IHS relative to a fixed substrate. These package handling loads may be experienced during heatsink removal.

Table 2-2. Package Handling Guidelines

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Maximum Recommended</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shear</td>
<td>70 lbs</td>
</tr>
<tr>
<td>Tensile</td>
<td>25 lbs</td>
</tr>
<tr>
<td>Torque</td>
<td>35 in.lbs</td>
</tr>
</tbody>
</table>

2.1.5 Package Insertion Specifications

The processor can be inserted into and removed from a LGA1366 socket 15 times. The socket should meet the LGA1366 requirements detailed in Section 5.
2.1.6 Processor Mass Specification

The typical mass of the processor is 35 grams. This mass [weight] includes all the components that are included in the package.

2.1.7 Processor Materials

Table 2-3 lists some of the package components and associated materials.

Table 2-3. Processor Materials

<table>
<thead>
<tr>
<th>Component</th>
<th>Material</th>
</tr>
</thead>
<tbody>
<tr>
<td>Integrated Heat Spreader (IHS)</td>
<td>Nickel Plated Copper</td>
</tr>
<tr>
<td>Substrate</td>
<td>Fiber Reinforced Resin</td>
</tr>
<tr>
<td>Substrate Lands</td>
<td>Gold Plated Copper</td>
</tr>
</tbody>
</table>

2.1.8 Processor Markings

Figure 2-4 shows the topside markings on the processor. This diagram is to aid in the identification of the processor.

Figure 2-4. Processor Top-Side Markings

Legend: Mark Text (Engineering Mark):
- GRP1LINE1: INTEL\{M\}\{C\}\{YY
- GRP1LINE2: INTEL CONFIDENTIAL
- GRP1LINE3: QDF ES XXXXX
- GRP1LINE4: FORECAST-NAME
- GRP1LINE5: \{FPO\} \{e4\}

Legend: Mark Text (Production Mark):
- GRP1LINE1: INTEL\{M\}\{C\}\{YY PROC#
- GRP1LINE2: SUB-BRAND
- GRP1LINE3: SSPEC XXXXX
- GRP1LINE4: SPEED/CACHE/INTC
- GRP1LINE5: \{FPO\} \{e4\}
2.1.9 Processor Land Coordinates

Figure 2-5 shows the bottom view of the processor land coordinates. The coordinates are referred to throughout the document to identify processor lands.

Figure 2-5. Processor Land Coordinates and Quadrants, Bottom View
This section describes a surface mount, LGA (Land Grid Array) socket intended for the Intel® Xeon® processor C5500/C3500 series in the Picket Post platform. The socket provides I/O, power and ground contacts. The socket contains 1366 contacts arrayed about a cavity in the center of the socket with lead-free solder balls for surface mounting on the motherboard.

The socket has 1366 contacts with 1.016 mm X 1.016 mm pitch (X by Y) in a 43 x 41 grid array with 21 x 17 grid depopulation in the center of the array and selective depopulation elsewhere.

The socket must be compatible with the package (processor) and the Independent Loading Mechanism (ILM). The design includes a back plate which is integral to having a uniform load on the socket solder joints. Socket loading specifications are listed in Section 5.

Figure 3-1. LGA1366 Socket with Pick and Place Cover Removed
Figure 3-2. LGA1366 Socket Contact Numbering (Top View of Socket)
3.1 Board Layout

The land pattern for the LGA1366 socket is 40 mils X 40 mils (X by Y), and the pad size is 18 mils. There is no round-off (conversion) error between socket pitch (1.016 mm) and board pitch (40 mil) because these values are equivalent.

In general, metal defined (MD) pads perform better than solder mask defined (SMD) pads under thermal cycling, and SMD pads perform better than MD pads under dynamic stress. Recommendations for pad definition on a per pad basis do not exist for the LGA1366 socket.

The 40 mil spacing results in a reduced drill keepout as compared to previous platforms. Drill keepout is explained in section 3.2.1 of the Intel® Xeon® 5500 Platform Design Guide (PDG). Select PCB suppliers are capable of producing 40 mil spacing.

Figure 3-3. LGA1366 Socket Land Pattern (Top View of Board)
3.2 Attachment to Motherboard

The socket is attached to the motherboard by 1366 solder balls. There are no additional external methods (i.e. screw, extra solder, adhesive, etc.) to attach the socket. As indicated in Figure 3-4, the Independent Loading Mechanism (ILM) is not present during the attach (reflow) process.

![Figure 3-4. Attachment to Motherboard](image)

3.3 Socket Components

The socket has two main components, the socket body and Pick and Place (PnP) cover, and is delivered as a single integral assembly. See Appendix C for detailed drawings.

3.3.1 Socket Body Housing

The housing material is thermoplastic or equivalent with UL 94 V-0 flame rating capable of withstanding 260°C for 40 seconds (typical reflow/rework). The socket coefficient of thermal expansion (in the XY plane), and creep properties, must be such that the integrity of the socket is maintained for the conditions listed in Section 8.

The color of the housing will be dark as compared to the solder balls. This provides the contrast needed for pick and place vision systems.

3.3.2 Solder Balls

A total of 1366 solder balls corresponding to the contacts are on the bottom of the socket for surface mounting with the motherboard.

The socket has the following solder ball material:

- Lead free SAC (SnAgCu) solder alloy with a silver (Ag) content between 3% and 4% and a melting temperature of approximately 217°C. The alloy must be compatible with immersion silver (ImAg) motherboard surface finish and a SAC alloy solder paste.

The co-planarity (profile) and true position requirements are defined in Appendix C.
3.3.3 Contacts

Base material for the contacts is high strength copper alloy.

For the area on socket contacts where processor lands will mate, there is a 0.381 μm [15 μinches] minimum gold plating over 1.27 μm [50 μinches] minimum nickel underplate.

No contamination by solder in the contact area is allowed during solder reflow.

3.3.4 Pick and Place Cover

The cover provides a planar surface for vacuum pick up used to place components in the Surface Mount Technology (SMT) manufacturing line. The cover remains on the socket during reflow to help prevent contamination during reflow. The cover can withstand 260° C for 40 seconds (typical reflow/ rework profile) and the conditions listed in Section 6 without degrading.

As indicated in Figure 3-5, the cover remains on the socket during ILM installation, and should remain on whenever possible to help prevent damage to the socket contacts.

Cover retention must be sufficient to support the socket weight during lifting, translation, and placement (board manufacturing), and during board and system shipping and handling.

The covers are designed to be interchangeable between socket suppliers. As indicated in Figure 3-5, a Pin1 indicator on the cover provides a visual reference for proper orientation with the socket.

Figure 3-5. Pick and Place Cover
3.4 Package Installation / Removal

As indicated in Figure 3-6, access is provided to facilitate manual installation and removal of the package.

To assist in package orientation and alignment with the socket:

- The package Pin1 triangle and the socket Pin1 chamfer provide visual reference for proper orientation.
- The package substrate has orientation notches along two opposing edges of the package, offset from the centerline. The socket has two corresponding orientation posts to physically prevent mis-orientation of the package. These orientation features also provide initial rough alignment of package to socket.
- The socket has alignment walls at the four corners to provide final alignment of the package.

Figure 3-6. Package Installation / Removal Features

3.4.1 Socket Standoffs and Package Seating Plane

Standoffs on the bottom of the socket base establish the minimum socket height after solder reflow and are specified in Appendix C.

Similarly, a seating plane on the topside of the socket establishes the minimum package height. See Section 5.2 for the calculated IHS height above the motherboard.
3.5 Durability

The socket must withstand 30 cycles of processor insertion and removal. The max chain contact resistance from Table 5-4 must be met when mated in the 1st and 30th cycles.

The socket Pick and Place cover must withstand 15 cycles of insertion and removal.

3.6 Markings

There are three markings on the socket:

- LGA1366: Font type is Helvetica Bold - minimum 6 point (2.125 mm).
- Manufacturer's insignia (font size at supplier's discretion).
- Lot identification code (allows traceability of manufacturing date and location).

All markings must withstand 260°C for 40 seconds (typical reflow/rework profile) without degrading, and must be visible after the socket is mounted on the motherboard.

LGA1366 and the manufacturer's insignia are molded or laser marked on the side wall.

3.7 Component Insertion Forces

Any actuation must meet or exceed SEMI S8-95 Safety Guidelines for Ergonomics/Human Factors Engineering of Semiconductor Manufacturing Equipment, example Table R2-7 (Maximum Grip Forces). The socket must be designed so that it requires no force to insert the package into the socket.

3.8 Socket Size

Socket information needed for motherboard design is given in Appendix C.

This information should be used in conjunction with the reference motherboard keep-out drawings provided in Appendix B to ensure compatibility with the reference thermal mechanical components.

3.9 LGA1366 Socket NCTF Solder Joints

Intel has defined selected solder joints of the socket as non-critical to function (NCTF) when evaluating package solder joints post environmental testing. The processor signals at NCTF locations are typically redundant ground or non-critical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality. Figure 3-7 identifies the NCTF solder joints.
Note: For platforms supporting the DP processor land C3 is CTF.
4 Independent Loading Mechanism (ILM)

The Independent Loading Mechanism (ILM) provides the force needed to seat the 1366-LGA land package onto the socket contacts. The ILM is physically separate from the socket body. The assembly of the ILM is expected to occur after wave solder. The exact assembly location is dependent on manufacturing preference and test flow. See the Manufacturing Advantage Service collateral for this platform for additional guidance.

**Note:** The ILM has two critical functions: deliver the force to seat the processor onto the socket contacts and distribute the resulting load evenly through the socket solder joints.

**Note:** The mechanical design of the ILM is integral to the overall functionality of the LGA1366 socket. Intel performs detailed studies on integration of processor package, socket and ILM as a system. These studies directly impact the design of the ILM. The Intel reference ILM will be “build to print” from Intel controlled drawings. Intel recommends using the Intel Reference ILM. Custom non-Intel ILM designs do not benefit from Intel’s detailed studies and may not incorporate critical design parameters.

4.1 Design Concept

The ILM consists of two assemblies that will be procured as a set from the enabled vendors. These two components are ILM cover assembly and back plate.

4.1.1 ILM Cover Assembly Design Overview

The ILM cover assembly consists of four major pieces: load lever, load plate, frame and the captive fasteners.

The load lever and load plate are stainless steel. The frame and fasteners are high carbon steel with appropriate plating. The fasteners are fabricated from a high carbon steel. The frame provides the hinge locations for the load lever and load plate.

The cover assembly design ensures that once assembled to the back plate and the load lever is closed, the only features touching the board are the captive fasteners. The nominal gap of the frame to the board is ~1 mm when the load plate is closed on the empty socket or when closed on the processor package.

When closed the load plate applies two point loads onto the IHS at the “dimpled” features shown in Figure 4-1. The reaction force from closing the load plate is transmitted to the frame and through the captive fasteners to the back plate. Some of the load is passed through the socket body to the board inducing a slight compression on the solder joints.
4.1.2 ILM Back Plate Design Overview

The unified back plate for 2-socket server and 2-socket Workstation products consists of a flat steel back plate with threaded studs for ILM attach, and internally threaded nuts for heatsink attach. The threaded studs have a smooth surface feature that provides alignment for the back plate to the motherboard for proper assembly of the ILM around the socket. A clearance hole is located at the center of the plate to allow access to test points and backside capacitors. An additional cut-out on two sides provides clearance for backside voltage regulator components. An insulator is pre-applied.

Back plates for processors in 1-socket workstation platforms are covered in the Intel® Xeon® Processor 3500 Series Thermal/Mechanical Design Guide.
4.2 Assembly of ILM to a Motherboard

The ILM design allows a bottoms up assembly of the components to the board. In step 1 (see Figure 4-3), the back plate is placed in a fixture. Holes in the motherboard provide alignment to the threaded studs. In step 2, the ILM cover assembly is placed over the socket and threaded studs. Using a T20 Torx* driver fasten the ILM cover assembly to the back plate with the four captive fasteners. Torque to 8 inch-pounds. The length of the threaded studs accommodate board thicknesses from 0.062” - 0.100”.

Figure 4-2. Back Plate
Figure 4-3. ILM Assembly

Step 1: With socket body refloked on board, and back plate in fixture, align board holes to back plate studs.

Step 2: With back plate against bottom of board, align ILM cover assembly to back plate studs.
As indicated in Figure 4-4, socket protrusion and ILM key features prevent 180-degree rotation of ILM cover assembly with respect to socket. The result is a specific Pin 1 orientation with respect to ILM lever.

See the Manufacturing Advantage Service for additional details on fixtures and assembly guidance.

**Figure 4-4. Pin1 and ILM Lever**
This chapter describes the electrical, mechanical and environmental specifications for the LGA1366 socket and the Independent Loading Mechanism.

### 5.1 Component Mass

**Table 5-1. Socket Component Mass**

<table>
<thead>
<tr>
<th>Component</th>
<th>Mass</th>
</tr>
</thead>
<tbody>
<tr>
<td>Socket body, contacts, and PnP cover</td>
<td>15 gm</td>
</tr>
<tr>
<td>ILM cover</td>
<td>43 gm</td>
</tr>
<tr>
<td>ILM back plate for dual processor server products</td>
<td>100 gm</td>
</tr>
</tbody>
</table>

**Notes:**
1. Preliminary guidance.

### 5.2 Package/Socket Stackup Height

**Table 5-2. 1366-land Package and LGA1366 Socket Stackup Height**

<table>
<thead>
<tr>
<th>Integrated stackup height (mm)</th>
<th>7.729 ± 0.282 mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>From top of board to top of IHS</td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**
1. This data is provided for information only, and should be derived from: (a) the height of the socket seating plane above the motherboard after reflow, given in Appendix C, (b) the height of the package, from the package seating plane to the top of the IHS, and accounting for its nominal variation and tolerances that are given in the corresponding processor Datasheet.
2. This value is a RSS calculation.

### 5.3 Socket Maximum Temperature

The power dissipated within the socket is a function of the current at the pin level and the effective pin resistance. To ensure socket long term reliability, Intel defines socket maximum temperature using a via on the underside of the motherboard. Exceeding the temperature guidance may result in socket body deformation, or increases in thermal and electrical resistance which can cause a thermal runaway and eventual electrical failure. The guidance for socket maximum temperature is listed below:

- Via temperature under socket < 96 °C

The specific via used for temperature measurement is located on the bottom of the motherboard between pins AY23, AY22, AW23, and AW22. See Figure 5-1.
The socket maximum temperature is defined at Thermal Design Current (TDC). In addition, the heatsink performance targets and boundary conditions of Table 6-1 must be met to limit power dissipation through the socket.

To measure via temperature:

1. Drill a hole through the back plate at the specific via defined above.

2. Thread a T-type thermocouple (36 - 40 gauge) through the hole and glue it into the specific via on the underside of the motherboard.

3. Once the glue dries, reinstall the back plate and measure the temperature.

**Figure 5-1. Socket Temperature Measurement Location**
5.4 Loading Specifications

The socket will be tested against the conditions listed in the LGA1366 Socket Validation Reports with heatsink and the ILM attached, under the loading conditions outlined in this chapter.

Table 5-3 provides load specifications for the LGA1366 socket with the ILM installed. The maximum limits should not be exceeded during heatsink assembly, shipping conditions, or standard use condition. Exceeding these limits during test may result in component failure. The socket body should not be used as a mechanical reference or load-bearing surface for thermal solutions.

Table 5-3. Socket and ILM Mechanical Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static compressive load from ILM cover to processor IHS</td>
<td>445 N [100 lbf]</td>
<td>623 N [140 lbf]</td>
<td>3, 4</td>
</tr>
<tr>
<td>Heatsink static compressive load</td>
<td>0 N [0 lbf]</td>
<td>266 N [60 lbf]</td>
<td>1, 2, 3</td>
</tr>
<tr>
<td>Total static compressive load (ILM plus Heatsink)</td>
<td>470 N (106 lbf)</td>
<td>890 N (200 lbf)</td>
<td>3, 4</td>
</tr>
<tr>
<td>Dynamic compressive load (with heatsink installed)</td>
<td>N/A</td>
<td>890 N [200 lbf]</td>
<td>1, 3, 5, 6</td>
</tr>
<tr>
<td>Pick &amp; place cover insertion / removal force</td>
<td>N/A</td>
<td>10.2 N [2.3 lbf]</td>
<td></td>
</tr>
<tr>
<td>Load lever actuation force</td>
<td>N/A</td>
<td>38.3 N [8.6 lbf] in the vertical direction, 10.2 N [2.3 lbf] in the lateral direction.</td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. These specifications apply to uniform compressive loading in a direction perpendicular to the IHS top surface.
2. This is the minimum and maximum static force that can be applied by the heatsink and it’s retention solution to maintain the heatsink to IHS interface. This does not imply the Intel reference TIM is validated to these limits.
3. Loading limits are for the LGA1366 socket.
4. This minimum limit defines the compressive force required to electrically seat the processor onto the socket contacts.
5. Dynamic loading is defined as an 11 ms duration average load superimposed on the static load requirement.
6. Test condition used a heatsink mass of 550gm [1.21 lb] with 50 g acceleration measured at heatsink mass. The dynamic portion of this specification in the product application can have flexibility in specific values, but the ultimate product of mass times acceleration should not exceed this dynamic load.

5.4.1 Board Deflection Guidance

See Intel® Xeon® Processor 5500 Series Thermal/Mechanical Design Guide (TMDG), Revision 2.1 for detailed board deflection guidance.
5.5 Electrical Requirements

LGA1366 socket electrical requirements are measured from the socket-seating plane of the processor to the component side of the socket PCB to which it is attached. All specifications are maximum values (unless otherwise stated) for a single socket contact, but includes effects of adjacent contacts where indicated.

Table 5-4. Electrical Requirements for LGA1366 Socket

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mated loop inductance, loop</td>
<td>&lt;3.9 nH</td>
<td>The inductance calculated for two contacts, considering one forward conductor and one return conductor. These values must be satisfied at the worst-case height of the socket.</td>
</tr>
<tr>
<td>Mated partial mutual inductance, L</td>
<td>NA</td>
<td>The inductance on a contact due to any single neighboring contact.</td>
</tr>
<tr>
<td>Maximum mutual capacitance, C</td>
<td>&lt;1 pF</td>
<td>The capacitance between two contacts.</td>
</tr>
<tr>
<td>Socket Average Contact Resistance (EOL)</td>
<td>15.2 mΩ</td>
<td>The socket average contact resistance target is derived from average of every chain contact resistance for each part used in testing, with a chain contact resistance defined as the resistance of each chain minus resistance of shorting bars divided by number of lands in the daisy chain. The specification listed is at room temperature and has to be satisfied at all time. <strong>Socket Contact Resistance:</strong> The resistance of the socket contact, solderball, and interface resistance to the interposer land.</td>
</tr>
<tr>
<td>Max Individual Contact Resistance (EOL)</td>
<td>≤ 100 mΩ</td>
<td>The specification listed is at room temperature and has to be satisfied at all time. <strong>Socket Contact Resistance:</strong> The resistance of the socket contact, solderball, and interface resistance to the interposer land; gaps included.</td>
</tr>
<tr>
<td>Bulk Resistance Increase</td>
<td>≤ 3 mΩ</td>
<td>The bulk resistance increase per contact from 24°C to 107°C. <strong>Socket Contact Resistance:</strong> The resistance of the socket contact, solderball, and interface resistance to the interposer land; gaps included.</td>
</tr>
<tr>
<td>Dielectric Withstand Voltage</td>
<td>360 Volts RMS</td>
<td></td>
</tr>
<tr>
<td>Insulation Resistance</td>
<td>800 MΩ</td>
<td></td>
</tr>
</tbody>
</table>
5.6 Environmental Requirements

Design, including materials, shall be consistent with the manufacture of units that meet the following environmental reference points.

The reliability targets in this section are based on the expected field use environment for these products. The test sequence for new sockets will be developed using the knowledge-based reliability evaluation methodology, which is acceleration factor dependent. A simplified process flow of this methodology can be seen in Figure 5-2.

**Figure 5-2. Flow Chart of Knowledge-Based Reliability Evaluation Methodology**

A detailed description of this methodology is at:

6 Thermal Specifications

6.1 Package Thermal Specifications

The Intel® Xeon® processor C5500/C3500 series requires a thermal solution to maintain temperatures within its operating limits. Any attempt to operate the processor outside these operating limits may result in permanent damage to the processor and potentially other components within the system. Maintaining the proper thermal environment is key to reliable, long-term system operation.

A complete solution includes both component and system level thermal management features. Component level thermal solutions can include active or passive heatsinks attached to the processor integrated heat spreader (IHS).

This section provides data necessary for developing a complete thermal solution. For more information on designing a component level thermal solution, see Section 7.

6.1.1 Thermal Specifications

To allow the optimal operation and long-term reliability of Intel processor-based systems, the processor must remain within the minimum and maximum case temperature (T_{CASE}) specifications as defined by the applicable thermal profile. Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system. These specifications are based on pre-silicon estimates. These specifications may be further updated as more data becomes available. Processors are listed here by TDP (Multiple SKUs may have the same TDP and same spec).

The Intel® Xeon® processor C5500/C3500 series implements a methodology for managing processor temperatures that is intended to support acoustic noise reduction through fan speed control and to assure processor reliability. Selection of the appropriate fan speed is based on the relative temperature data reported by the processor's Platform Environment Control Interface (PECI) as described in Section 6.3. If PECI is less than TCONTROL, then the case temperature is permitted to exceed the Thermal Profile, but PECI must remain at or below TCONTROL. If PECI \geq TCONTROL, then the case temperature must meet the Thermal Profile. The temperature reported over PECI is always a negative value and represents a delta below the onset of thermal control circuit (TCC) activation, as indicated by PROCHOT# (see Section 6.2, Processor Thermal Features). Systems that implement fan speed control must be designed to use this data. Systems that do not alter the fan speed only need to guarantee the case temperature meets the thermal profile specifications.

The Intel® Xeon® processor EC5500 and EC3500 series (85 W and 65 W) supports a single Thermal Profile. See specifications below. For this processor, it is expected that the Thermal Control Circuit (TCC) would only be activated for very brief periods of time when running the most power-intensive applications.

The Intel® Celeron® processor P1053 (30 W) (see specifications below) supports a single Thermal Profile. For this processor, it is expected that the Thermal Control Circuit (TCC) would only be activated for very brief periods of time when running the most power-intensive applications.
The Intel® Xeon® processor LC5500 and LC3500 series (60 W, 48 W, 35 W, and 23 W) all support Thermal Profiles with nominal and short-term conditions designed to meet NEBS Level 3 compliance. See specifications below. For these SKUs, operation at either the nominal or short-term thermal profiles should result in virtually no TCC activation.

Analysis indicates that real applications are unlikely to cause the processor to consume maximum power dissipation for sustained time periods. Intel recommends that complete thermal solution designs target the Thermal Design Power (TDP), instead of the maximum processor power consumption. The Adaptive Thermal Monitor feature is intended to help protect the processor in the event that an application exceeds the TDP recommendation for a sustained time period. For more details on this feature, see Section 6.2. The Adaptive Thermal Monitor feature must be enabled for the processor to remain within its specifications.

Table 6-1. Intel® Xeon® Processor EC5549 and EC5509 Thermal Specifications

<table>
<thead>
<tr>
<th>Core Frequency</th>
<th>Thermal Design Power (W)</th>
<th>Minimum TCASE (°C)</th>
<th>Maximum TCASE (°C)</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Launch to FMB</td>
<td>85</td>
<td>5</td>
<td></td>
<td>1, 2, 3, 4, 5</td>
</tr>
</tbody>
</table>

Notes:
1. These values are specified at VCC_MAX for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static VCC and ICC combination wherein VCC exceeds VCC_MAX at specified ICC. See the loadline specifications in theDatasheet.
2. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum TCASE.
3. These specifications are based on initial silicon characterization. These specifications may be further updated as more characterization data becomes available.
4. Power specifications are defined at all VIDs found in the Datasheet. The Intel® Xeon® processor C5500/ C3500 series may be shipped under multiple VIDs for each frequency.
5. FMB (Flexible Motherboard) guidelines provide a design target for meeting all planned processor frequency requirements.

Figure 6-1. Intel® Xeon® Processor EC5549 and EC5509 Thermal Profile

Notes:
1. Intel® Xeon® processor EC5549 and EC5509 Thermal Profile is representative of a volumetrically unconstrained platform. See Table 6-2 for discrete points that constitute the thermal profile.
2. Implementation of Intel® Xeon® processor EC5549 and EC5509 Thermal Profile should result in virtually no TCC activation.
### Thermal Specifications

#### Table 6-2. Intel® Xeon® Processor EC5549 and EC5509 Thermal Profile

<table>
<thead>
<tr>
<th>Power (W)</th>
<th>$T_{CASE_MAX} \ (^{\circ}C)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>51.8</td>
</tr>
<tr>
<td>5</td>
<td>53.3</td>
</tr>
<tr>
<td>10</td>
<td>54.8</td>
</tr>
<tr>
<td>15</td>
<td>56.3</td>
</tr>
<tr>
<td>20</td>
<td>57.9</td>
</tr>
<tr>
<td>25</td>
<td>59.4</td>
</tr>
<tr>
<td>30</td>
<td>60.9</td>
</tr>
<tr>
<td>35</td>
<td>62.4</td>
</tr>
<tr>
<td>40</td>
<td>63.9</td>
</tr>
<tr>
<td>45</td>
<td>65.4</td>
</tr>
<tr>
<td>50</td>
<td>67.0</td>
</tr>
<tr>
<td>55</td>
<td>68.5</td>
</tr>
<tr>
<td>60</td>
<td>70.0</td>
</tr>
<tr>
<td>65</td>
<td>71.5</td>
</tr>
<tr>
<td>70</td>
<td>73.0</td>
</tr>
<tr>
<td>75</td>
<td>74.5</td>
</tr>
<tr>
<td>80</td>
<td>76.0</td>
</tr>
<tr>
<td>85</td>
<td>77.6</td>
</tr>
</tbody>
</table>

#### Table 6-3. Intel® Xeon® Processor EC3539 and EC5539 Thermal Specifications

<table>
<thead>
<tr>
<th>Core Frequency</th>
<th>Thermal Design Power (W)</th>
<th>Minimum $T_{CASE}$ (°C)</th>
<th>Maximum $T_{CASE}$ (°C)</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Launch to FMB</td>
<td>65</td>
<td>5</td>
<td>See Figure 6-2; Table 6-4</td>
<td>1, 2, 3, 4, 5</td>
</tr>
</tbody>
</table>

### Notes:
1. These values are specified at $V_{CC\_MAX}$ for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static $V_{CC}$ and $I_{CC}$ combination wherein $V_{CC}$ exceeds $V_{CC\_MAX}$ at specified $I_{CC}$. See the loadline specifications in the Datasheet.
2. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum $T_{CASE}$. 
3. These specifications are based on initial silicon characterization. These specifications may be further updated as more characterization data becomes available.
4. Power specifications are defined at all VIDs found in the Datasheet. The Intel® Xeon® processor C5500/C3500 series Intel® Xeon® processor C5500/C3500 series may be shipped under multiple VIDs for each frequency.
5. FMB (Flexible Motherboard) guidelines provide a design target for meeting all planned processor frequency requirements.
Figure 6-2. Intel® Xeon® Processor EC3539 and EC5539 Thermal Profile

![Thermal Profile Graph]

**Notes:**
1. Intel® Xeon® processor EC3539 and EC5539 Thermal Profile is representative of a volumetrically unconstrained platform. See Table 6-4 for discrete points that constitute the thermal profile.
2. Implementation of Intel® Xeon® processor EC3539 and EC5539 Thermal Profile should result in virtually no TCC activation.

Table 6-4. Intel® Xeon® Processor EC3539 and EC5539 Thermal Profile

<table>
<thead>
<tr>
<th>Power (W)</th>
<th>T(_{\text{CASE Max}}) (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>55.0</td>
</tr>
<tr>
<td>5</td>
<td>56.5</td>
</tr>
<tr>
<td>10</td>
<td>58.0</td>
</tr>
<tr>
<td>15</td>
<td>59.5</td>
</tr>
<tr>
<td>20</td>
<td>61.0</td>
</tr>
<tr>
<td>25</td>
<td>62.6</td>
</tr>
<tr>
<td>30</td>
<td>64.1</td>
</tr>
<tr>
<td>35</td>
<td>65.6</td>
</tr>
<tr>
<td>40</td>
<td>67.1</td>
</tr>
<tr>
<td>45</td>
<td>68.6</td>
</tr>
<tr>
<td>50</td>
<td>70.1</td>
</tr>
<tr>
<td>55</td>
<td>71.6</td>
</tr>
<tr>
<td>60</td>
<td>73.1</td>
</tr>
<tr>
<td>65</td>
<td>74.6</td>
</tr>
</tbody>
</table>
Thermal Specifications

Table 6-5. Intel® Xeon® Processor LC5528 Thermal Specifications

<table>
<thead>
<tr>
<th>Core Frequency</th>
<th>Thermal Design Power (W)</th>
<th>Minimum TCASE (°C)</th>
<th>Maximum TCASE (°C)</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Launch to FMB</td>
<td>60</td>
<td>5</td>
<td>See Figure 6-3; Table 6-6</td>
<td>1, 2, 3, 4, 5</td>
</tr>
</tbody>
</table>

Notes:
1. These values are specified at VCC_MAX for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static VCC and ICC combination wherein VCC exceeds VCC_MAX at specified ICC. See the loadline specifications in the Datasheet.
2. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum TCASE.
3. These specifications are based on initial silicon characterization. These specifications may be further updated as more characterization data becomes available.
4. Power specifications are defined at all VIDs found in the Datasheet. The Intel® Xeon® processor C5500/ C3500 series may be shipped under multiple VIDs for each frequency.
5. FMB (Flexible Motherboard) guidelines provide a design target for meeting all planned processor frequency requirements.

Figure 6-3. Intel® Xeon® Processor LC5528 Thermal Profile

Notes:
1. Intel® Xeon® processor LC5528 Thermal Profile is representative of a volumetrically constrained platform. See Table 6-7 for discrete points that constitute the thermal profile.
2. Implementation of Intel® Xeon® processor LC5528 nominal and short-term thermal profiles should result in virtually no TCC activation. Furthermore, utilization of thermal solutions that do not meet this Thermal Profile will result in increased probability of TCC activation and may incur measurable performance loss.
3. The Nominal Thermal Profile must be used for all normal operating conditions, or for products that do not require NEBS Level 3 compliance.
4. The Short-Term Thermal Profile may only be used for short-term excursions to higher ambient operating temperatures, not to exceed 360 hours per year. Operation at the Short-Term Thermal Profile for durations exceeding 360 hours per year violate the processor thermal specifications and may result in permanent damage to the processor.
### Table 6-6. Intel® Xeon® Processor LC5528 Thermal Profile

<table>
<thead>
<tr>
<th>Power (W)</th>
<th>Nominal $T_{CASE_MAX}$ (°C)</th>
<th>Short-term $T_{CASE_MAX}$ (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>51.9</td>
<td>66.9</td>
</tr>
<tr>
<td>5</td>
<td>53.4</td>
<td>68.4</td>
</tr>
<tr>
<td>10</td>
<td>54.9</td>
<td>69.9</td>
</tr>
<tr>
<td>15</td>
<td>56.4</td>
<td>71.4</td>
</tr>
<tr>
<td>20</td>
<td>57.9</td>
<td>72.9</td>
</tr>
<tr>
<td>25</td>
<td>59.5</td>
<td>74.5</td>
</tr>
<tr>
<td>30</td>
<td>61.0</td>
<td>76.0</td>
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<td>25</td>
<td>62.5</td>
<td>77.5</td>
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<tr>
<td>40</td>
<td>64.0</td>
<td>79.0</td>
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<td>45</td>
<td>65.5</td>
<td>80.5</td>
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<tr>
<td>50</td>
<td>67.0</td>
<td>82.0</td>
</tr>
<tr>
<td>55</td>
<td>68.5</td>
<td>83.5</td>
</tr>
<tr>
<td>60</td>
<td>70.0</td>
<td>85.0</td>
</tr>
</tbody>
</table>

### Table 6-7. Intel® Xeon® Processor LC5518 Thermal Specifications

<table>
<thead>
<tr>
<th>Core Frequency</th>
<th>Thermal Design Power (W)</th>
<th>Minimum $T_{CASE}$ (°C)</th>
<th>Maximum $T_{CASE}$ (°C)</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Launch to FMB</td>
<td>48</td>
<td>5</td>
<td>See Figure 6-4; Table 6-8</td>
<td>1, 2, 3, 4, 5</td>
</tr>
</tbody>
</table>

**Notes:**

1. These values are specified at $V_{CC\_MAX}$ for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static $V_{CC}$ and $I_{CC}$ combination wherein $V_{CC}$ exceeds $V_{CC\_MAX}$ at specified ICC. See the loadline specifications in the Datasheet.
2. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum $T_{CASE}$.
3. These specifications are based on initial silicon characterization. These specifications may be further updated as more characterization data becomes available.
4. Power specifications are defined at all VIDs found in the Datasheet. The Intel® Xeon® processor C5500/C3500 series may be shipped under multiple VIDs for each frequency.
5. FMB (Flexible Motherboard) guidelines provide a design target for meeting all planned processor frequency requirements.
Notes:
1. Intel® Xeon® processor LC5518 Thermal Profile is representative of a volumetrically constrained platform. See Table 6-8 for discrete points that constitute the thermal profile.
2. Implementation of Intel® Xeon® processor LC5518 nominal and short-term thermal profiles should result in virtually no TCC activation. Furthermore, utilization of thermal solutions that do not meet this Thermal Profile will result in increased probability of TCC activation and may incur measurable performance loss.
3. The Nominal Thermal Profile must be used for all normal operating conditions, or for products that do not require NEBS Level 3 compliance.
4. The Short-Term Thermal Profile may only be used for short-term excursions to higher ambient operating temperatures, not to exceed 360 hours per year, as compliant with NEBS Level 3. Operation at the Short-Term Thermal Profile for durations exceeding 360 hours per year violate the processor thermal specifications and may result in permanent damage to the processor.

Table 6-8. Intel® Xeon® Processor LC5518 Thermal Profile

<table>
<thead>
<tr>
<th>Power (W)</th>
<th>Nominal T(_{\text{CASE_MAX}}) (°C)</th>
<th>Short-term T(_{\text{CASE_MAX}}) (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>52.0</td>
<td>67.0</td>
</tr>
<tr>
<td>5</td>
<td>54.7</td>
<td>69.7</td>
</tr>
<tr>
<td>10</td>
<td>57.3</td>
<td>72.3</td>
</tr>
<tr>
<td>15</td>
<td>60.0</td>
<td>75.0</td>
</tr>
<tr>
<td>20</td>
<td>62.6</td>
<td>77.6</td>
</tr>
<tr>
<td>25</td>
<td>65.3</td>
<td>80.3</td>
</tr>
<tr>
<td>30</td>
<td>68.0</td>
<td>83.0</td>
</tr>
<tr>
<td>35</td>
<td>70.6</td>
<td>85.6</td>
</tr>
<tr>
<td>40</td>
<td>73.3</td>
<td>88.3</td>
</tr>
<tr>
<td>48</td>
<td>77.5</td>
<td>92.5</td>
</tr>
</tbody>
</table>
1. These values are specified at VCC_MAX for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static VCC and ICC combination wherein VCC exceeds VCC_MAX at specified ICC. See the loadline specifications in the Datasheet.

2. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum TCASE.

3. These specifications are based on initial silicon characterization. These specifications may be further updated as more characterization data becomes available.

4. Power specifications are defined at all VIDs found in the Datasheet. The Intel® Xeon® processor C5500/C3500 series may be shipped under multiple VIDs for each frequency.

5. FMB (Flexible Motherboard) guidelines provide a design target for meeting all planned processor frequency requirements.

Table 6-9. Intel® Celeron® Processor P1053 Thermal Specifications

<table>
<thead>
<tr>
<th>Core Frequency</th>
<th>Thermal Design Power (W)</th>
<th>Minimum TCASE (°C)</th>
<th>Maximum TCASE (°C)</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Launch to FMB</td>
<td>30</td>
<td>5</td>
<td>See Figure 6-5; Table 6-10</td>
<td>1, 2, 3, 4, 5</td>
</tr>
</tbody>
</table>

Notes:

1. Intel® Celeron® processor P1053 Thermal Profile is representative of a volumetrically unconstrained platform. See Table 6-12 for discrete points that constitute the thermal profile.

2. Implementation of Intel® Celeron® processor P1053 Thermal Profile should result in virtually no TCC activation.

Table 6-10. Intel® Celeron® Processor P1053 Thermal Profile

<table>
<thead>
<tr>
<th>Power (W)</th>
<th>TCASE_MAX (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>55.0</td>
</tr>
<tr>
<td>5</td>
<td>56.6</td>
</tr>
<tr>
<td>10</td>
<td>58.1</td>
</tr>
<tr>
<td>15</td>
<td>59.7</td>
</tr>
<tr>
<td>20</td>
<td>61.3</td>
</tr>
<tr>
<td>25</td>
<td>62.8</td>
</tr>
<tr>
<td>30</td>
<td>64.4</td>
</tr>
</tbody>
</table>
Thermal Specifications

Table 6-11. Intel® Xeon® Processor LC3528 Thermal Specifications

<table>
<thead>
<tr>
<th>Core Frequency</th>
<th>Thermal Design Power (W)</th>
<th>Minimum TCASE (°C)</th>
<th>Maximum TCASE (°C)</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Launch to FMB</td>
<td>35</td>
<td>5</td>
<td>See Figure 6-6; Table 6-12</td>
<td>1, 2, 3, 4, 5</td>
</tr>
</tbody>
</table>

Notes:
1. These values are specified at VCC_MAX for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static VCC and ICC combination wherein VCC exceeds VCC_MAX at specified ICC. See the loadline specifications in the Datasheet.
2. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum TCASE.
3. These specifications are based on initial silicon characterization. These specifications may be further updated as more characterization data becomes available.
4. Power specifications are defined at all VIDs found in the Datasheet. The Intel® Xeon® processor C5500/C3500 series may be shipped under multiple VIDs for each frequency.
5. FMB (Flexible Motherboard) guidelines provide a design target for meeting all planned processor frequency requirements.

Figure 6-6. Intel® Xeon® Processor LC3528 Thermal Profile

Notes:
1. Intel® Xeon® processor LC3528 Thermal Profile is representative of a volumetrically constrained platform. See Table 6-12 for discrete points that constitute the thermal profile.
2. Implementation of Intel® Xeon® processor LC3528 nominal and short-term thermal profiles should result in virtually no TCC activation. Furthermore, utilization of thermal solutions that do not meet this Thermal Profile will result in increased probability of TCC activation and may incur measurable performance loss.
3. The Nominal Thermal Profile must be used for all normal operating conditions, or for products that do not require NEBS Level 3 compliance.
4. The Short-Term Thermal Profile may only be used for short-term excursions to higher ambient operating temperatures, not to exceed 96 hours per instance, 360 hours per year, and a maximum of 15 instances per year, as compliant with NEBS Level 3. Operation at the Short-Term Thermal Profile for durations exceeding 360 hours per year violate the processor thermal specifications and may result in permanent damage to the processor.
Table 6-12. Intel® Xeon® Processor LC3528 Thermal Profile

<table>
<thead>
<tr>
<th>Power (W)</th>
<th>Nominal T_{CASE,MAX} (°C)</th>
<th>Short-term T_{CASE,MAX} (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>45.0</td>
<td>60.0</td>
</tr>
<tr>
<td>5</td>
<td>49.9</td>
<td>64.9</td>
</tr>
<tr>
<td>10</td>
<td>54.7</td>
<td>69.7</td>
</tr>
<tr>
<td>15</td>
<td>59.6</td>
<td>74.6</td>
</tr>
<tr>
<td>20</td>
<td>64.4</td>
<td>79.4</td>
</tr>
<tr>
<td>25</td>
<td>69.3</td>
<td>84.3</td>
</tr>
<tr>
<td>30</td>
<td>74.1</td>
<td>89.1</td>
</tr>
<tr>
<td>35</td>
<td>79.0</td>
<td>94.0</td>
</tr>
</tbody>
</table>

Table 6-13. Intel® Xeon® Processor LC3518 Thermal Specifications

<table>
<thead>
<tr>
<th>Core Frequency</th>
<th>Thermal Design Power (W)</th>
<th>Minimum T_{CASE} (°C)</th>
<th>Maximum T_{CASE} (°C)</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Launch to FMB</td>
<td>23</td>
<td>5</td>
<td>See Figure 6-7; Table 6-14</td>
<td>1, 2, 3, 4, 5</td>
</tr>
</tbody>
</table>

Notes:
1. These values are specified at V_{CC,MAX} for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC,MAX} at specified I_{CC}. See the loadline specifications in the Datasheet.
2. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum T_{CASE}.
3. These specifications are based on initial silicon characterization. These specifications may be further updated as more characterization data becomes available.
4. Power specifications are defined at all VIDs found in the Datasheet. The Intel® Xeon® processor C5500/ C3500 series may be shipped under multiple VIDs for each frequency.
5. FMB (Flexible Motherboard) guidelines provide a design target for meeting all planned processor frequency requirements.
**Notes:**

1. Intel® Xeon® processor LC3518 Thermal Profile is representative of a volumetrically constrained platform. See Table 6-14 for discrete points that constitute the thermal profile.
2. Implementation of Intel® Xeon® processor LC3518 nominal and short-term thermal profiles should result in virtually no TCC activation. Furthermore, utilization of thermal solutions that do not meet this Thermal Profile will result in increased probability of TCC activation and may incur measurable performance loss.
3. The Nominal Thermal Profile must be used for all normal operating conditions, or for products that do not require NEBS Level 3 compliance.
4. The Short-Term Thermal Profile may only be used for short-term excursions to higher ambient temperatures, not to exceed 360 hours per year, as compliant with NEBS Level 3. Operation at the Short-Term Thermal Profile for durations exceeding 360 hours per year violate the processor thermal specifications and may result in permanent damage to the processor.

**Table 6-14. Intel® Xeon® Processor LC3518 Thermal Profile**

<table>
<thead>
<tr>
<th>Power (W)</th>
<th>Nominal T\text{CASE_MAX} (°C)</th>
<th>Short-term T\text{CASE_MAX} (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>45.0</td>
<td>60.0</td>
</tr>
<tr>
<td>5</td>
<td>52.5</td>
<td>67.5</td>
</tr>
<tr>
<td>10</td>
<td>60.0</td>
<td>75.0</td>
</tr>
<tr>
<td>15</td>
<td>67.5</td>
<td>82.5</td>
</tr>
<tr>
<td>20</td>
<td>75.0</td>
<td>90.0</td>
</tr>
<tr>
<td>23</td>
<td>79.5</td>
<td>94.5</td>
</tr>
</tbody>
</table>
6.1.2 Thermal Metrology

The minimum and maximum case temperatures ($T_{CASE}$) are specified in Thermal Profiles above and are measured at the geometric top center of the TTV integrated heat spreader (IHS). Figure 6-8 illustrates the location where $T_{CASE}$ temperature measurements should be made.

**Figure 6-8. TTV Case Temperature ($T_{CASE}$) Measurement Location**

---

**Notes:**

1. Figure is not to scale and is for reference only.
2. B1: Max = 45.07 mm, Min = 44.93 mm.
3. B2: Max = 42.57 mm, Min = 42.43 mm.
4. C1: Max = 39.1 mm, Min = 38.9 mm.
5. C2: Max = 36.6 mm, Min = 36.4 mm.
6. C3: Max = 2.3 mm, Min = 2.2 mm.
7. C4: Max = 2.3 mm, Min = 2.2 mm.
6.2 Processor Thermal Features

6.2.1 Processor Temperature

A new feature in the Intel® Xeon® processor C5500/C3500 series is a software readable field in the IA32_TEMPERATURE_TARGET register that contains the minimum temperature at which the TCC will be activated and PROCHOT# will be asserted. The TCC activation temperature is calibrated on a part-by-part basis and normal factory variation may result in the actual TCC activation temperature being higher than the value listed in the register. TCC activation temperatures may change based on processor stepping, frequency or manufacturing efficiencies.

Note: There is no specified correlation between DTS temperatures and processor case temperatures; therefore it is not possible to use this feature to ensure the processor case temperature meets the Thermal Profile specifications.

6.2.2 Adaptive Thermal Monitor

The Adaptive Thermal Monitor feature provides an enhanced method for controlling the processor temperature when the processor silicon reaches its maximum operating temperature. Adaptive Thermal Monitor uses Thermal Control Circuit (TCC) activation to reduce processor power via a combination of methods. The first method (Frequency/VID control) involves the processor adjusting its operating frequency (via the core ratio multiplier) and input voltage (via the VID signals). This combination of reduced frequency and VID results in a reduction to the processor power consumption. The second method (clock modulation) reduces power consumption by modulating (starting and stopping) the internal processor core clocks. The processor intelligently selects the appropriate TCC method to use on a dynamic basis. BIOS is not required to select a specific method (as with previous-generation processors supporting TM1 or TM2).

The Adaptive Thermal Monitor feature must be enabled for the processor to be operating within specifications. The temperature at which Adaptive Thermal Monitor activates the Thermal Control Circuit is not user configurable and is not software visible. Snooping and interrupt processing are performed in the normal manner while the TCC is active.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss, and in some cases may result in a T_{CASE} that exceeds the specified maximum temperature and may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under-designed may not be capable of cooling the processor even when the TCC is active continuously.

The duty cycle for the TCC, when activated by the Thermal Monitor, is factory configured and cannot be modified. The Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines.

The following sections provide more details on the different TCC mechanisms used by the Intel® Xeon® processor C5500/C3500 series.
6.2.2.1 Frequency/VID Control

The processor uses Frequency/VID control whereby TCC activation causes the processor to adjust its operating frequency (via the core ratio multiplier) and input voltage (via the VID signals). This combination of reduced frequency and VID results in a reduction to the processor power consumption.

This method includes multiple operating points, each consisting of a specific operating frequency and voltage. The first operating point represents the normal operating condition for the processor. The remaining points consist of both lower operating frequencies and voltages. When the TCC is activated, the processor automatically transitions to the new operating frequency. This transition occurs very rapidly (on the order of 2 microseconds).

Once the new operating frequency is engaged, the processor will transition to the new core operating voltage by issuing a new VID code to the voltage regulator. The voltage regulator must support dynamic VID steps to support this method. During the voltage change, it will be necessary to transition through multiple VID codes to reach the target operating voltage. Each step will be one VID table entry (see the Intel® Xeon® Processor C5500/C3500 Series Datasheet). The processor continues to execute instructions during the voltage transition. Operation at the lower voltages reduces the power consumption of the processor.

A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the operating frequency and voltage transition back to the normal system operating point via the intermediate VID/frequency points. Transition of the VID code will occur first, to insure proper operation once the processor reaches its normal operating frequency. Refer to Figure 6-9 for an illustration of this ordering.

Figure 6-9. Frequency and Voltage Ordering
6.2.2.2 Clock Modulation

Clock modulation is performed by alternately turning the clocks off and on at a duty cycle specific to the processor (factory configured to 37.5% on and 62.5% off). The period of the duty cycle is configured to 32 microseconds when the TCC is active. Cycle times are independent of processor frequency. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the TCC goes inactive and clock modulation ceases. Clock modulation is automatically engaged as part of the TCC activation when the Frequency/VID targets are at their minimum settings. It may also be initiated by software at a configurable duty cycle.

6.2.2.3 On-Demand Mode

The processor provides an auxiliary mechanism that allows system software to force the processor to reduce its power consumption. This mechanism is referred to as "On-Demand" mode and is distinct from the Adaptive Thermal Monitor feature. On-Demand mode is intended as a means to reduce system level power consumption. Systems utilizing the Intel® Xeon® Processor 5500 Series must not rely on software usage of this mechanism to limit the processor temperature. If bit 4 of the IA32_CLOCK_MODULATION MSR is set to a ‘1’, the processor will immediately reduce its power consumption via modulation (starting and stopping) of the internal core clock, independent of the processor temperature. When using On-Demand mode, the duty cycle of the clock modulation is programmable via bits 3:1 of the same IA32_CLOCK_MODULATION MSR. In On-Demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off to 87.5% on/12.5% off in 12.5% increments. On-Demand mode may be used in conjunction with the Adaptive Thermal Monitor; however, if the system tries to enable On-Demand mode at the same time the TCC is engaged, the factory configured duty cycle of the TCC will override the duty cycle selected by the On-Demand mode.

6.2.2.4 PROCHOT# Signal

An external signal, PROCHOT# (processor hot), is asserted when the processor core temperature has reached its maximum operating temperature. If Adaptive Thermal Monitor is enabled (it must be enabled for the processor to be operating within specification), the TCC will be active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT#.

The PROCHOT# signal is bi-directional in that it can either signal when the processor (any core) has reached its maximum operating temperature or be driven from an external source to activate the TCC. The ability to activate the TCC via PROCHOT# can provide a means for thermal protection of system components.

As an output, PROCHOT# will go active when the processor temperature monitoring sensor detects that one or more cores has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. As an input, assertion of PROCHOT# by the system will activate the TCC for all cores. TCC activation when PROCHOT# is asserted by the system will result in the processor immediately transitioning to the minimum frequency and corresponding voltage (using Freq/VID control). Clock modulation is not activated in this case. The TCC will remain active until the system de-asserts PROCHOT#.
PROCHOT# can allow VR thermal designs to target maximum sustained current instead of maximum current. Systems should still provide proper cooling for the VR, and rely on PROCHOT# only as a backup in case of system cooling failure. The system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its Thermal Design Power.

With a properly designed and characterized thermal solution, it is anticipated that PROCHOT# will only be asserted for very short periods of time when running the most power intensive applications. An under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may cause a noticeable performance loss. Refer to the appropriate platform design guide and for details on implementing the bi-directional PROCHOT# feature.

6.2.3 THERMTRIP# Signal

Regardless of whether or not Adaptive Thermal Monitor is enabled, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached an elevated temperature (see the THERMTRIP# definition in the Datasheet). At this point, the THERMTRIP# signal will go active and stay active as described in the Datasheet. THERMTRIP# activation is independent of processor activity. If THERMTRIP# is asserted, processor core voltage (VCC) must be removed within the timeframe defined in the Datasheet. The temperature at which THERMTRIP# asserts is not user configurable and is not software visible.

6.3 Platform Environment Control Interface (PECI)

6.3.1 Introduction

The Platform Environment Control Interface (PECI) is a one-wire interface that provides a communication channel between Intel processor and chipset components to external monitoring devices. The processor implements a PECI interface to allow communication of processor thermal and other information to other devices on the platform. The processor provides a digital thermal sensor (DTS) on each core for fan speed control. The DTS is calibrated at the factory to provide a digital representation of processor temperature relative PROCHOT# assertion. Instantaneous temperature readings from the DTS are available via the IA32_TEMP_STATUS MSR; averaged DTS values are read via the PECI interface.

The PECI physical layer is a self-clocked one-wire bus that begins each bit with a driven, rising edge from an idle level near zero volts. The duration of the signal driven high depends on whether the bit value is a logic '0' or logic '1'. PECI also includes variable data transfer rate established with every message. The single wire interface provides low board routing overhead for the multiple load connections in the congested routing area near the processor and chipset components. Bus speed, error checking, and low protocol overhead provides adequate link bandwidth and reliability to transfer critical device operating conditions and configuration information.

6.3.1.1 Fan Speed Control with Digital Thermal Sensor

Fan speed control solutions use a value stored in the static variable, TCONTROL. The DTS temperature data which is delivered over PECI (in response to a GetTemp0() command) is compared to this TCONTROL reference. The DTS temperature is reported as a relative value versus an absolute value. The temperature reported over PECI is
always a negative value and represents a delta below the onset of thermal control circuit (TCC) activation, as indicated by PROCHOT#. Therefore, as the temperature approaches TCC activation, the value approaches zero degrees.

### 6.3.1.2 Processor Thermal Data Sample Rate and Filtering

The processor digital thermal sensor (DTS) provides an improved capability to monitor device hot spots, which inherently leads to more varying temperature readings over short time intervals. To reduce the sample rate requirements on PECI and improve thermal data stability vs. time the processor DTS implements an averaging algorithm that filters the incoming data. This filter is expressed mathematically as:

\[
\text{PECI}(t) = \text{PECI}(t-1) + \frac{1}{(2^X)} \times \left[ \text{Temp} - \text{PECI}(t-1) \right]
\]

Where: PECI(t) is the new averaged temperature, PECI(t-1) is the previous averaged temperature Temp is the raw temperature data from the DTS, X is the Thermal Averaging Constant (TAC).

**Note:** Only values read via the PECI interface are averaged. Temperature values read via the IA32_TEMP_STATUS MSR are not averaged.

The Thermal Averaging Constant is a BIOS configurable value that determines the time in milliseconds over which the DTS temperature values are averaged. Short averaging times will make the averaged temperature values respond more quickly to DTS changes. Long averaging times will result in better overall thermal smoothing but also incur a larger time lag between fast DST temperature changes and the value read via PECI.

Within the processor, the DTS converts an analog signal into a digital value representing the temperature relative to TCC activation. The conversions are in integers with each single number change corresponding to approximately 1° C. DTS values reported via the internal processor MSR will be in whole integers.

As a result of the averaging function described above, DTS values reported over PECI will include a 6-bit fractional value. Under typical operating conditions, where the temperature is close to Tcontrol, the fractional values may not be of interest. But when the temperature approaches zero, the fractional values can be used to detect the activation of the TCC. An averaged temperature value between 0 and 1 can only occur if the TCC has been activated during the averaging window. As TCC activation time increases, the fractional value will approach zero. Fan control circuits can detect this situation and take appropriate action as determined by the system designers. Of course, fan control chips can also monitor the Prochot pin to detect TCC activation via a dedicated input pin on the package.
6.3.2 PECI Specifications

6.3.2.1 PECI Device Address

The processor PECI_ID# signal is used to configure the PECI address for the given processor. The PECI register resides at:

- Address 30h when PECI_ID# is pulled to Vtt.
- Address 31h when PECI_ID# is terminated to ground.

6.3.2.2 PECI Command Support

PECI commands are in the Intel® Xeon® Processor C5500/C3500 Series Datasheet).

6.3.2.3 PECI Fault Handling Requirements

PECI is largely a fault tolerant interface, including noise immunity and error checking improvements over other comparable industry standard interfaces. The PECI client is as reliable as the device that it is embedded in, and thus given operating conditions that fall under the specification, the PECI will always respond to requests and the protocol itself can be relied upon to detect any transmission failures. There are, however, certain scenarios in which the PECI is known to be unresponsive. Before a power on RESET# and during RESET# assertion, PECI is not ensured to provide reliable thermal data. System designs should implement a default power-on condition that ensures proper processor operation during the time frame when reliable data is not available via PECI.

To protect platforms from potential operational or safety issues due to an abnormal condition on PECI, the Host controller should take action to protect the system from possible damaging states. If the Host controller cannot complete a valid PECI transactions of GetTemp0() with a given PECI device over three consecutive failed transactions or a one second max specified interval, then it should take appropriate actions to protect the corresponding device and/or other system components from overheating. The Host controller may also implement an alert to software in the event of a critical or continuous fault condition.

6.3.2.4 PECI GetTemp0() Error Code Support

The error codes supported for the processor GetTemp0() command are listed in Table 6-15.

<table>
<thead>
<tr>
<th>Error Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8000h</td>
<td>General sensor error</td>
</tr>
</tbody>
</table>

§
This section describes 1U and ATCA reference heatsinks. These heatsink designs target the Intel® Xeon® processor C5500/C3500 series and thermal design guidelines for the processor.

### 7.1 Performance Targets

Table 7-1 provides boundary conditions and performance targets for 1U and ATCA heatsinks. These values are used to generate processor thermal specifications and to provide guidance for heatsink design. Other Intel® Xeon® Processor 5500 Series thermal solutions may work with the same retention. See the Intel® Xeon® Processor 5500 Series Thermal/Mechanical Design Guide.

**Note:** Custom heatsinks and high airflow ATCA designs can cool higher power processors than typical ATCA.

Table 7-1. Boundary Conditions and Performance Targets

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Altitude, system ambient temp</td>
<td>Sea level, 40°C</td>
</tr>
<tr>
<td>TDP</td>
<td>85 W, 65 W, 30 W, 60 W, 48 W, 35 W</td>
</tr>
<tr>
<td>$T_{LA}^{1,4}$</td>
<td>52°C, 55°C, 55°C, 52/67°C, 52/67°C, 45/60°C</td>
</tr>
<tr>
<td>$\Psi_{CA}^{2}$</td>
<td>0.303°C/W, 0.302°C/W, 0.313°C/W, 0.302°C/W, 0.532°C/W, 0.970°C/W</td>
</tr>
<tr>
<td>System form factor$^3$</td>
<td>1U, 1U, 1U, 1U or ATCA, ATCA, ATCA or Dense Blade</td>
</tr>
<tr>
<td>Heatsink volumetric</td>
<td>90 x 90 x 27 mm (1U), 1U or Custom ATCA, 90 x 90 x 13 mm, 90 x 90 x 13 mm</td>
</tr>
<tr>
<td>Heatsink technology$^5$</td>
<td>Cu base, Al fins, Cu base, Cu fins</td>
</tr>
</tbody>
</table>

**Note:**
1. Local ambient temperature of the air entering the heatsink.
2. Max target (mean + 3σ) for thermal characterization parameter (Section 7.5.1).
3. Reference system configuration. Processors are not limited to these form factors.
4. Local Ambient Temperature written 45/60°C means 45°C under Nominal conditions but 60°C is allowed for Short-Term NEBS excursions.
5. Passive heatsinks with TIM.
For a 1U reference heatsink, see Appendix B for detailed drawings. Table 7-1 specifies Ψ_{CA} target at 11 CFM through the fins. Figure 7-1 shows Ψ_{CA} and pressure drop for the 1U heatsink versus the airflow provided. Best-fit equations are provided to prevent errors associated with reading the graph.

**Figure 7-1. 1U Heatsink Performance Curves**

<table>
<thead>
<tr>
<th>CFM Through Fins</th>
<th>Ψ_{CA}, C/W</th>
<th>ΔP, inch water</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
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<tr>
<td>50</td>
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</table>

Mean Ψ_{CA} = 0.1430 + 1.141*CFM^{0.817}

σ = 0.0016 C/W

ΔP = 1.9e-04CFM^{2} + 2.0e-02CFM

Intel® Xeon® Processor C5500/C3500 Series and LGA1366 Socket
Thermal/Mechanical Design Guide
August 2010
Order Number: 323107-002US
For the ATCA reference heatsink, see Appendix B for detailed drawings. Table 7-1 specifies $\Psi_{ca}$ target at 30 CFM per blade. Figure 7-2 shows $\Psi_{ca}$ and pressure drop for the ATCA heatsink versus the airflow provided. Best-fit equations are provided to prevent errors associated with reading the graph.

Figure 7-2. ATCA Heatsink Performance Curves

![ATCA Heatsink Performance Curves](image)

$\Delta P = 1.3 \times 10^{-4} \text{ CFM}^2 + 1.1 \times 10^{-2} \text{ CFM}$

Mean $\Psi_{ca} = 0.337 + 1.625 \times \text{CFM} - 0.939$

7.2 Heat Pipe Considerations

Figure 7-3 shows the orientation and position of the TTV die. The TTV die is sized and positioned similar to the processor die.
7.3 Assembly

Figure 7-4. 1U Reference Heatsink Assembly

[Diagram of 1U Reference Heatsink Assembly with labels for 1U Reference Heatsink, Captive Screw, Thermal Interface Material: Honeywell PCM45F, IHS: Integrated Heat Spreader, Threaded Nut, Reference Back Plate (Unified Back Plate)]
The assembly process for the 1U reference heatsink begins with application of Honeywell* PCM45F thermal interface material to improve conduction from the IHS. Tape and roll format is recommended. Pad size is 35 x 35mm.

Next, the heatsink is positioned such that the heatsink fins are parallel to system airflow. While lowering the heatsink onto the IHS, the four captive screws of the heatsink are aligned to the four threaded nuts of the back plate.

Using a #2 Phillips driver, torque the four captive screws to 8 inch-pounds.

This assembly process is designed to produce a static load of 39 - 51 lbf, for 0.062" - 0.100" board thickness respectively. Honeywell PCM45F is expected to meet the performance targets in Table 7-1 from 30 - 60 lbf. From Table 5-3, the Heatsink Static Compressive Load of 0 - 60 lbf allows for designs that vary from the 1U reference heatsink. Example: A customer’s unique heatsink with very little static load (as little as 0 lbf) is acceptable from a socket loading perspective as long as the TCASE specification is met.

Compliance to board keepout zones in Appendix B is assumed for this assembly process.

7.3.1 Thermal Interface Material (TIM)

TIM should be verified to be within its recommended shelf life before use. Surfaces should be free of foreign materials prior to application of TIM. Use isopropyl alcohol and a lint-free cloth to remove old TIM before applying new TIM.

7.4 Structural Considerations

The mass of the 1U and ATCA reference heatsinks does not exceed 500 gm.

From Table 5-3, the Dynamic Compressive Load of 200 lbf max allows for designs that exceed 500 gm as long as the mathematical product does not exceed 200 lbf. Example: A heatsink of 2lb mass (908 gm) x 50 g (acceleration) x 2.0 Dynamic Amplification Factor = 200 lbf. The Total Static Compressive Load (Table 5-3) should also be considered in dynamic assessments.

The heatsink limit of 500 gm and use of back plate have eliminated the need for Direct Chassis Attach retention (as used with previous Dual-Core Intel® Xeon® processor 5000 sequence). Direct contact between back plate and chassis pan will help minimize board deflection during shock.

Placement of board-to-chassis mounting holes also impacts board deflection and resultant socket solder ball stress. Customers need to assess shock for their designs as their heatsink retention (back plate), heatsink mass and chassis mounting holes may vary.
### 7.5 Thermal Design

#### 7.5.1 Thermal Characterization Parameter

The case-to-local ambient Thermal Characterization Parameter ($\Psi_{CA}$) is defined by:

**Equation 7-1.**

$$\Psi_{CA} = \frac{(T_{CASE} - T_{LA})}{TDP}$$

Where:

- $T_{CASE} =$ Processor case temperature (°C). For $T_{CASE}$ specification see Section 6.
- $T_{LA} =$ Local ambient temperature in chassis at processor (°C).
- $TDP =$ TDP (W) assumes all power dissipates through the integrated heat spreader. This inexact assumption is convenient for heatsink design. TTVs are often used to dissipate TDP. Correction offsets account for differences in temperature distribution between processor and TTV.

**Equation 7-2.**

$$\Psi_{CA} = \Psi_{CS} + \Psi_{SA}$$

Where:

- $\Psi_{CS} =$ Thermal characterization parameter of the TIM (°C/W) is dependent on the thermal conductivity and thickness of the TIM.
- $\Psi_{SA} =$ Thermal characterization parameter from heatsink-to-local ambient (°C/W) is dependent on the thermal conductivity and geometry of the heatsink and dependent on the air velocity through the heatsink fins.

Figure 7-5 illustrates the thermal characterization parameters.

**Figure 7-5. Processor Thermal Characterization Parameter Relationships**

![Processor Thermal Characterization Parameter Relationships Diagram]
### 7.5.2 NEBS Thermal Profile

Processors that offer a NEBS thermal profile are specified in the *Intel® Xeon® Processor C5500/C3500 Series Datasheet)*.

NEBS thermal profiles help relieve thermal constraints for Short-Term NEBS conditions. To help reliability, processors must meet the nominal thermal profile under standard operating conditions and can only rise up to the Short-Term spec for NEBS excursions (see Figure 7-6). Short-Term is clearly defined for NEBS Level 3 but the 360 hours per year limit is a key consideration.

**Note:** Fan speed can be decreased and case temperatures can be allowed to rise above the thermal profile if the processor is below Tcontrol (see Section 7.6.1). Exceeding the thermal profile at these lower temperatures is not considered a risk to reliability.

**Figure 7-6. NEBS Thermal Profile**

![Thermal Profile Graph](image)

**Note:**

1.) The thermal specifications shown in this graph are for reference only. See the *Intel® Xeon® Processor C5500/C3500 Series Datasheet* for the Thermal Profile specifications. In case of conflict, the data information in the Datasheet supersedes any data in this figure.

2.) The Nominal Thermal Profile must be used for all normal operating conditions, or for products that do not require NEBS Level 3 compliance.

3.) The Short-Term Thermal Profile may only be used for short-term excursions to higher ambient operating temperatures, not to exceed 360 hours per year as compliant with NEBS Level 3.

4.) Implementation of either thermal profile should result in virtually no TCC activation.

5.) Utilization of a thermal solution that exceeds the Short-Term Thermal Profile, or which operates at the Short-Term Thermal Profile for a duration longer than the limits specified in Note 3 above, do not meet the processor thermal specifications and may result in permanent damage to the processor.
7.5.3 **Power Thermal Utility**

The Intel® Xeon® processor C5500/C3500 series Power Thermal Utility allows power and thermal testing of the processor.

The Utility will allow power and thermal testing of the processor. The thermal solution must be designed to keep the processor Tcase within specification for the Thermal Design Power (TDP) as specified in Section 6. Contact your Intel representative to obtain the latest revision of the PTU.

The default power level from the drop down list represents TDP.

7.6 **Thermal Features**

More information regarding processor thermal features is contained in the appropriate Datasheet.

7.6.1 **Fan Speed Control**

There are many ways to implement fan speed control. Using processor ambient temperature (in addition to Digital Thermal Sensor) to scale fan speed with ambient temperature can improve acoustics when DTS > TCONTROL.

<table>
<thead>
<tr>
<th>Condition</th>
<th>FSC Scheme</th>
</tr>
</thead>
<tbody>
<tr>
<td>DTS ≤ TCONTROL</td>
<td>FSC can adjust fan speed to maintain DTS ≤ TCONTROL (low acoustic region).</td>
</tr>
<tr>
<td>DTS &gt; TCONTROL</td>
<td>FSC should adjust fan speed to keep TCASE at or below the Thermal Profile specification (increased acoustic region).</td>
</tr>
</tbody>
</table>

7.6.1.1 **TCONTROL Guidance**

Factory configured TCONTROL values are available in the appropriate Dear Customer Letter or may be extracted by issuing a Mailbox or an RDMSR instruction. See the appropriate Electrical, Mechanical, and Thermal Specifications (EMTS) for more information.
7.6.2 PECI Averaging and Catastrophic Thermal Management

By averaging DTS over PECI, thermal solution failure can be detected and a soft shutdown can be initiated to help prevent loss of data.

Thermal data is averaged over a rolling window of 256mS by default (X=8):

\[
\text{AVGN} = \text{AVGN}_{-1} \times (1 - 1/2^X) + \text{Temperature} \times 1/2^X
\]

Using a smaller averaging constant could cause premature detection of failure.

The Critical Temperature threshold generally triggers somewhere between PECI of -0.75 and -0.50. To avoid false shutdowns, initiate soft shutdown at -0.25.

Since customer designs, boundary conditions, and failure scenarios differ, above guidance should be tested in the customer’s system to prevent loss of data during shutdown.

7.6.3 Intel® Turbo Boost Technology

Intel® Turbo Boost Technology (Intel® TBT) is a new feature available on certain processor SKUs that opportunistically, and automatically, allows the processor to run faster than the marked frequency if the part is operating below its power, temperature and current limits.

Heatsink performance (lower \(\Psi_{CA}\) as described in Section 7.5.1) is one of several factors that can impact the amount of Intel® TBT frequency benefit. Intel® TBT performance is also constrained by ICC, and VCC limits.
Increased IMON accuracy may provide more Intel® TBT benefit on TDP limited applications, as compared to lower $\Psi_{CA}$, as temperature is not typically the limiter for these workloads. See Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.1 Design Guidelines for more information regarding IMON accuracy.

With Intel® TBT enabled, the processor may run more consistently at higher power levels (but still within TDP), and be more likely to operate above $T_{\text{CONTROL}}$, as compared to when Intel® TBT is disabled. This may result in higher acoustics.

7.6.4 Absolute Processor Temperature

Intel does not test any third-party software that reports absolute processor temperature. As such, Intel cannot recommend the use of software that claims this capability. Since there is part-to-part variation in the TCC (thermal control circuit) activation temperature, use of software that reports absolute temperature can be misleading.

See Section 6.2.1 for details regarding use of IA32_TEMPERATURE_TARGET register to determine the minimum absolute temperature at which the TCC will be activated and PROCHOT# will be asserted.

7.6.5 Custom Heat Sinks For UP ATCA

The embedded-specific 60W SKU was targeted for NEBS compliant 1U+ systems and UP ATCA configurations with custom thermal solutions. In order to cool this part in a single wide ATCA slot, a custom thermal solution will be required. Unique solutions like the UP ATCA processor will be very configuration specific so, the thermal solution for UP ATCA was not fully designed with retention and keep-out definitions. Figure 7-7 is a good example of a custom thermal solution for the UP ATCA processor.

To cool the additional power of a 60 W processor in ATCA, the heatsink volume had to grow. The assumption was that the heat sink could not grow wider because of VR and Memory placement so a Remote Heat Exchanger (RHE) was used. The RHE is attached to the main heat sink with a heat pipe. The RHE gives additional convective surface area and gives the thermal solution access to more air. Samples of the following design were ordered and tested for thermal performance only.

Flotherm analysis shows that the following design can cool an LGA1366 TTV in an ATCA blade at 30 CFM. The heat sink $\Psi_{ca}$ would be 0.50°C/W at 55°C ambient which falls below the thermal profile for the 60W processor.
Figure 7-7. UP ATCA Thermal Solution

Note: Thermal sample only, retention not production ready.

Figure 7-8. UP ATCA System Layout

Note: Heatsink should be optimized for the layout.
Figure 7-9. UP ATCA Heat Sink Drawing
8 Quality and Reliability Requirements

8.1 Use Conditions

Intel evaluates reliability performance based on the use conditions (operating environment) of the end product by using acceleration models.

The use condition environment definitions provided in Table 8-1 and Table 8-2 are based on speculative use condition assumptions, and are provided only as examples.

Table 8-1. Server Use Conditions Environment (System Level)

<table>
<thead>
<tr>
<th>Use Environment</th>
<th>Speculative Stress Condition</th>
<th>Example Use Condition</th>
<th>Example 7-Yr Stress Equiv.</th>
<th>Example 10-Yr Stress Equiv.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slow small internal gradient changes due to external ambient (temperature cycle or externally heated), Fast, large gradient on/off to max operating temp. (power cycle or internally heated including power save features)</td>
<td>Temperature Cycle ( \Delta T = 35 - 44^\circ C ) (solder joint)</td>
<td>550-930 cycles Temp Cycle Q (-25(^\circ) C to 100(^\circ) C)</td>
<td>780-1345 cycles Temp Cycle Q (-25(^\circ) C to 100(^\circ) C)</td>
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<tr>
<td>High ambient moisture during low-power state (operating voltage)</td>
<td>THB/HAST ( T = 25 - 30^\circ C ) 85% RH (ambient)</td>
<td>110-220 hrs at 110(^\circ) C 85% RH</td>
<td>145-240 hrs at 110(^\circ) C 85% RH</td>
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<tr>
<td>High operating temperature and short duration high temperature exposures</td>
<td>Bake ( T = 95 - 105^\circ C ) (contact)</td>
<td>700 – 2500 hrs at 125(^\circ) C</td>
<td>800 – 3300 hrs at 125(^\circ) C</td>
<td></td>
</tr>
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</table>
8.2 Intel Reference Component Validation

Intel tests reference components individually and as an assembly on mechanical test boards and assesses performance to the envelopes specified in previous sections by varying boundary conditions.

While component validation shows a reference design is tenable for a limited range of conditions, customers need to assess their specific boundary conditions and perform reliability testing based on their use conditions.

Intel reference components are also used in board functional tests to assess performance for specific conditions.

**Note:** The 1U thermal solution was tested but the ATCA solution was not fully tested.

### 8.2.1 Board Functional Test Sequence

Each test sequence should start with components (baseboard, heatsink assembly, and so on) that have not been previously submitted to any reliability testing.

The test sequence should always start with a visual inspection after assembly, and BIOS/Processor/memory test. The stress test should be then followed by a visual inspection and then BIOS/Processor/memory test.
8.2.2 Post-Test Pass Criteria

The post-test pass criteria are:

- No significant physical damage to the heatsink and retention hardware.
- Heatsink remains seated and its bottom remains mated flat against the IHS surface. No visible gap between the heatsink base and processor IHS. No visible tilt of the heatsink with respect to the retention hardware.
- No signs of physical damage on baseboard surface due to impact of heatsink.
- No visible physical damage to the processor package.
- Successful BIOS/processor/memory test of post-test samples.
- Thermal compliance testing to demonstrate that the case temperature specification can be met.

8.2.3 Recommended BIOS/Processor/Memory Test Procedures

This test ensures proper operation of the product before and after environmental stresses, with the thermal mechanical enabling components assembled. The test shall be conducted on a fully operational baseboard that has not been exposed to any battery of tests prior to the test being considered.

Test setup should include the following components, properly assembled and/or connected:

- Appropriate system baseboard.
- Processor and memory.
- All enabling components, including socket and thermal solution parts.

The pass criterion is that the system under test shall successfully complete the checking of BIOS, basic processor functions, and memory, without any errors. Intel PC Diags is an example of software that can be utilized for this test.

8.3 Material and Recycling Requirements

Material shall be resistant to fungal growth. Examples of non-resistant materials include cellulose materials, animal and vegetable based adhesives, grease, oils, and many hydrocarbons. Synthetic materials such as PVC formulations, certain polyurethane compositions (for example, polyester and some polyethers), plastics which contain organic fillers of laminating materials, paints, and varnishes also are susceptible to fungal growth. If materials are not fungal growth resistant, then MIL-STD-810E, Method 508.4 must be performed to determine material performance.

Any plastic component exceeding 25 gm should be recyclable per the European Blue Angel recycling standards.

The following definitions apply to the use of the terms lead-free, Pb-free, and RoHS compliant.

Lead-free and Pb-free: Lead has not been intentionally added, but lead may still exist as an impurity below 1000 ppm.
RoHS compliant: Lead and other materials banned in RoHS Directive are either (1) below all applicable substance thresholds as proposed by the EU or (2) an approved/pending exemption applies.

Note: RoHS implementation details are not fully defined and may change.
The part numbers below represent Intel reference designs and collaborative designs for 1U and ATCA heatsinks. These components are still in development and might not meet the criteria in Section 8. Customer implementation of these components may be unique and require validation by the customer. Customers can obtain these components directly from the suppliers below.

### Table A-1. Heatsinks and Thermal Interface Material

<table>
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<th>Component</th>
<th>Description</th>
<th>Supplier PN</th>
<th>Supplier Contact Info</th>
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<td><strong>1U Reference Heatsink</strong></td>
<td>1U Aluminum Fin, Copper Base</td>
<td>Fujikura</td>
<td>Fujikura America</td>
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<tr>
<td>p/n E32409-001</td>
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<td>HSA-8078 Rev A</td>
<td>Yuji Yasuda</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td><a href="mailto:yuji@fujikura.com">yuji@fujikura.com</a></td>
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<td></td>
<td></td>
<td>408-988-7478</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Fujikura Taiwan Branch</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Yao-Hsien Huang</td>
</tr>
<tr>
<td></td>
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<td><a href="mailto:yeohsien@fujikuratw.com.tw">yeohsien@fujikuratw.com.tw</a></td>
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<tr>
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<td></td>
<td>886(2)8788-4959</td>
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<tr>
<td><strong>ATCA Reference heatsink</strong></td>
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<td><strong>Thermal Interface Material</strong></td>
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<td>Scott Miller</td>
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<td>Paula Knoll</td>
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<td><a href="mailto:paula_knoll@honeywell.com">paula_knoll@honeywell.com</a></td>
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**Note:** Performance targets for heatsinks are described in Section 7.1. Mechanical drawings are provided in Appendix B. Mechanical models are listed in Table 1-1. Heatsinks assemble to server back plate (Table A-2).
Table A-2. LGA1366 Socket and ILM Components

<table>
<thead>
<tr>
<th>Item</th>
<th>Intel PN</th>
<th>Foxconn</th>
<th>Tyco</th>
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<td>ILM Cover Assembly</td>
<td>D92428-002</td>
<td>PT44L12-4101</td>
<td>1939738-1</td>
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<td>Server Back Plate</td>
<td>D92433-002</td>
<td>PT44P12-4101</td>
<td>1981467-1</td>
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<td>LGA1366 Socket</td>
<td>D86205-002</td>
<td>PE136627-4371-01F</td>
<td>1939737-1 or 1981837-1</td>
</tr>
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</table>

Supplier Contact Info
- Julia Jiang
  juliaj@foxconn.com
  408-919-6178
- Billy Hsieh
  billy.hsieh@tycoelectronics.com
  +81 44 844 8292

Note: The LGA1366 socket and ILM components are described in Section 2 and Section 3, respectively. Socket mechanical drawings are provided in Appendix B. Mechanical models are listed in Table 1-1.
### Table B-1. Mechanical Drawing List

<table>
<thead>
<tr>
<th>Description</th>
<th>Figure</th>
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</thead>
<tbody>
<tr>
<td>Board Keepin / Keepout Zones (Sheet 1 of 4)</td>
<td>Figure B-1</td>
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<tr>
<td>Board Keepin / Keepout Zones (Sheet 2 of 4)</td>
<td>Figure B-2</td>
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<td>Board Keepin / Keepout Zones (Sheet 3 of 4)</td>
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<tr>
<td>Board Keepin / Keepout Zones (Sheet 4 of 4)</td>
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<td>1U Reference Heatsink Assembly (Sheet 1 of 2)</td>
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<td>Heatsink Shoulder Screw (1U, 2U, and Tower)</td>
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<td>Heatsink Compression Spring (1U, 2U, and Tower)</td>
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<td>Heatsink Retaining Ring (1U, 2U, and Tower)</td>
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<tr>
<td>Heatsink Load Cup (1U, 2U, and Tower)</td>
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<td>Figure B-13</td>
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<td>ATCA Reference Heatsink Fin and Base (Sheet 2 of 2)</td>
<td>Figure B-16</td>
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Figure B-1. Board Keepin / Keepout Zones (Sheet 1 of 4)
Figure B-2. Board Keepin / Keepout Zones (Sheet 2 of 4)
Figure B-3. Board Keepin / Keepout Zones (Sheet 3 of 4)
Figure B-5. 1U Reference Heat Sink Assembly (Sheet 1 of 2)
Figure B-6. 1U Reference Heatsink Assembly (Sheet 2 of 2)
Figure B-8. 1U Reference Heatsink Fin and Base (Sheet 2 of 2)
Figure B-9. Heatsink Shoulder Screw (1U, 2U, and Tower)
Figure B-10. Heatsink Compression Spring (1U, 2U, and Tower)
Figure B-11. Heatsink Retaining Ring (1U, 2U, and Tower)
Figure B-12. Heatsink Load Cup (1U, 2U, and Tower)
Figure B-14. ATCA Reference Heatsink Assembly (Sheet 2 of 2)
Figure B-15. ATCA Reference Heatsink Fin and Base (Sheet 1 of 2)
Figure B-16. ATCA Reference Heatsink Fin and Base (Sheet 2 of 2)
Table C-1 lists the mechanical drawings included in this appendix.

<table>
<thead>
<tr>
<th>Drawing Description</th>
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<tr>
<td>&quot;Socket Mechanical Drawing - (Sheet 1 of 4)&quot;</td>
<td>Figure C-1</td>
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<td>&quot;Socket Mechanical Drawing - (Sheet 2 of 4)&quot;</td>
<td>Figure C-2</td>
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<td>&quot;Socket Mechanical Drawing - (Sheet 3 of 4)&quot;</td>
<td>Figure C-3</td>
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<tr>
<td>&quot;Socket Mechanical Drawing - (Sheet 4 of 4)&quot;</td>
<td>Figure C-4</td>
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</table>
Figure C-1. Socket Mechanical Drawing - (Sheet 1 of 4)
Figure C-3.  Socket Mechanical Drawing - (Sheet 3 of 4)