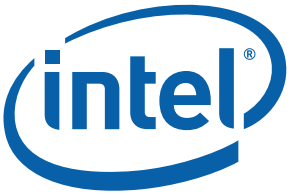

Intel® Xeon® Processor E7-2800/4800/8800 v2 Product Family

Boundary Scan Descriptor Language (BSDL) Readme

February 2014

Reference Number.: 329598-001

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Revision History

Document Number	Revision Number	Description	Date
329598	001	• Initial Release	February 2014

Overview

Scope

This document is intended for the development of IEEE 1149 Boundary Scan Tests for the Intel® Xeon® Processor E7-2800/4800/8800 v2 Product Family. This Readme assumes a working knowledge of IEEE 1149 methodologies and the In Circuit Test (ICT) manufacturing test methods.

This release package supports the processor steppings shown in the table below.

Table 1. BSDL File Summary

• IVB_EX_D1.bsdl • IVB_EX_C0.bsdl • IVB_EX_B3.bsdl • IVB_EX_B0.bsdl • IVB_EX_A0.bsdl	Full Boundary Scan File
• IVB_EX_D1_partial.bsdl • IVB_EX_C0_partial.bsdl • IVX_EX_B3_partial.bsdl	The respective BSDL files with a shortened boundary-scan chain due to the excluded Intel® Scalable Memory Interconnect (Intel® SMI) 2 pins
• IVB_EX_BSCAN_INIT.txt	The initialization sequence needed to enable partial BSCAN operation.

Related Documents

Refer to the following documents for additional processor information.

Table 2. Related Documents

Document	Document Number/Location
IEEE Standard Test Access Port and Boundary Scan Architecture Specification	http://standards.ieee.org

Readme

Full Boundary-Scan

After applying voltage to the power pins, the following initialization sequence must be completed prior to TAP accesses during application of the boundary-scan test patterns:

a. BCLK[1:0]_D[P/N] continuous toggle at 100 MHz

b. VMSE_PWR_OK, PWRGOOD, RESET_N are initialized LOW.

c. All power supplies are up.

d. VMSE_PWR_OK is driven HIGH and remains driven HIGH for the duration of the boundary-scan test pattern execution

e. EAR_N pin is initialized HIGH.

f. PROCHOT_N pin is initialized HIGH.

g. EAR_N and PROCHOT_N need to be initialized HIGH (de-asserted) prior to PWRGOOD assertion

h. PWRGOOD pin must be driven HIGH 2 ms after power pins are stable and remain drive HIGH for the duration of the boundary-scan test pattern execution.

i. RESET_N pin should be driven LOW for the duration of the boundary-scan test pattern execution.

Partial Boundary-Scan

The partial boundary-scan is necessary due to a known issue with theIntel® Xeon® Processor E7-2800/4800/8800 v2 Product Family which is described below:

Problem: A full function Boundary-scan operation requires a continuous running BCLK[1:0], however in some cases a partial BSDL file is needed where a continuous BCLK is not supplied. Also, The processor has limitation where if a full reset sequence is not applied, the PCU will not power up the Intel® Scalable Memory Interconnect (Intel® SMI) 2 domain so Intel SMI2 Boundary Scan is not available.

Implication: In cases where designs cannot do full a power-on during board manufacturing, the boundary-scan operation can cover all other pins with the partial BSDL file and the initialization sequence from the IVB_EX_BSCAN_INIT.txt file.

Workaround: A workaround to this is to enable Partial Boundary-scan functionality. If a continuous BCLK[1:0] cannot be supplied, BSCAN functionality can still be enabled with the exception of the Intel SMI2 pins. To enable this mode, the initialization sequence described below needs to be applied prior to the boundary-scan operation.

After applying voltage to power pins, the following initialization sequence must be completed prior to the first TAP accesses during application of the boundary scan test patterns:

a. VMSE_PWR_OK, PWRGOOD, RESET_N are initialized low.

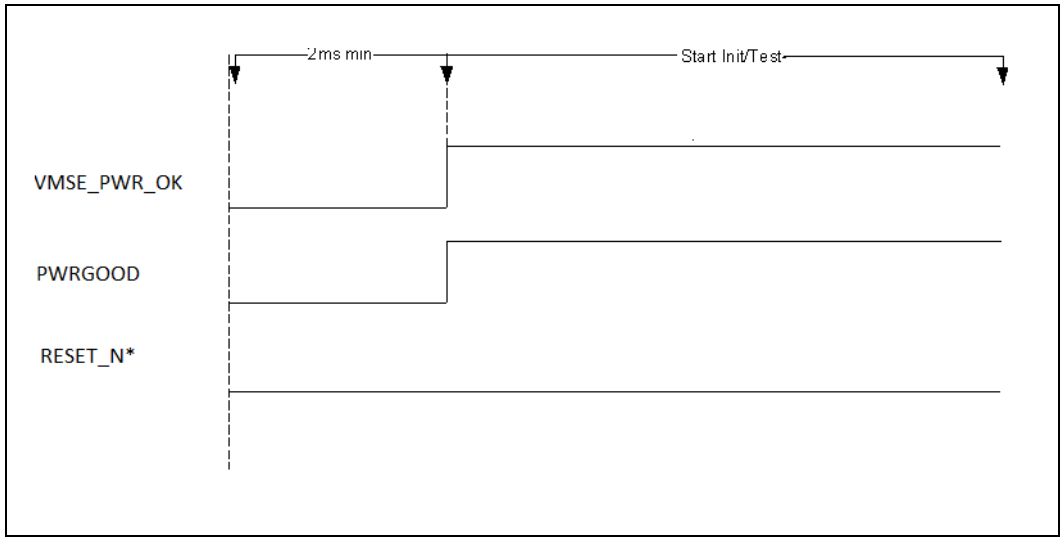
b. All power supplies are up.

c. VMSE_PWR_OK is driven HIGH and remains driven HIGH for the duration of the boundary-scan test pattern execution.

d. PWRGOOD pin must be driven HIGH 2 ms after power pins are stable and remain driven HIGH for the duration of the boundary-scan test pattern execution.

e. RESET_N pin should be driven LOW for the duration of the boundary-scan test pattern generation.

Figure 1. Reset Sequence



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