How to calculate the frequency, phase shift and duty cycle for clocking ALTLVDS soft SERDES using external PLL mode

Altera® devices have two types of implementation for SERDES blocks - hard SERDES and soft SERDES (built from logic cells). This document will discuss how to calculate the frequency, phase shift and duty cycle for each of the clocks needed for the external PLL interface with soft SERDES. The calculations will be verified by comparing to the settings from the Quartus® II software v11.0 Fitter report when using the internal PLL to interface with soft SERDES. By default, the ALTLVDS megafunction will infer the PLL and set the clocks based on the parameters you set (referred to as "internal" PLL in this document). By selecting external PLL mode, you must set the PLL parameters, but you can access other features of the PLL such as clock switchover, PLL reconfiguration, and other output clocks which would otherwise not be available when using the internal PLL.

1. Set Up

The examples in this document use the following:

- Quartus II software v11.0
- Cyclone® IV devices

2. Different modes of external PLL interface with soft SERDES

In the external PLL interface with soft SERDES, there are 4 modes which will have different calculation methods as following:

- LVDS TX with odd serialization factor
- LVDS TX with even serialization factor
- LVDS RX with odd deserialization factor
- LVDS RX with even deserialization factor

Notes:

a. The input port names for the ALTLVDS TX and RX might be different from device to device. The port names such as tx_inclock and tx_syncclock used in this document are the port naming used by ALTLVDS for Cyclone IV devices.
b. All the phase shifts are set for an edge aligned interface.

3. LVDS TX with odd serialization factor

For LVDS TX with odd serialization factor, Table 3-1 shows the interface clocks needed between the external PLL and the soft SERDES together with their calculations. Figure 3-1 shows an example of the connections between the external PLL and the ALTLVDS TX.

Note:

a. The inputs need to be pre-registered in the logic feeding the transmitter with the slow clock.

PLL output clocks	Soft SERDES
Fast clock – to tx_inclock	Frequency = data rate / 2 Phase shift = -180/2 = -90 Duty cycle = 50%
Slow clock – to tx_syncclock	Frequency = [data rate / SERDES factor] / 2 Phase shift = [-180 / SERDES factor] / 2 Duty cycle = 50%

Table 3-1. Calculations for LVDS TX with odd serialization factor

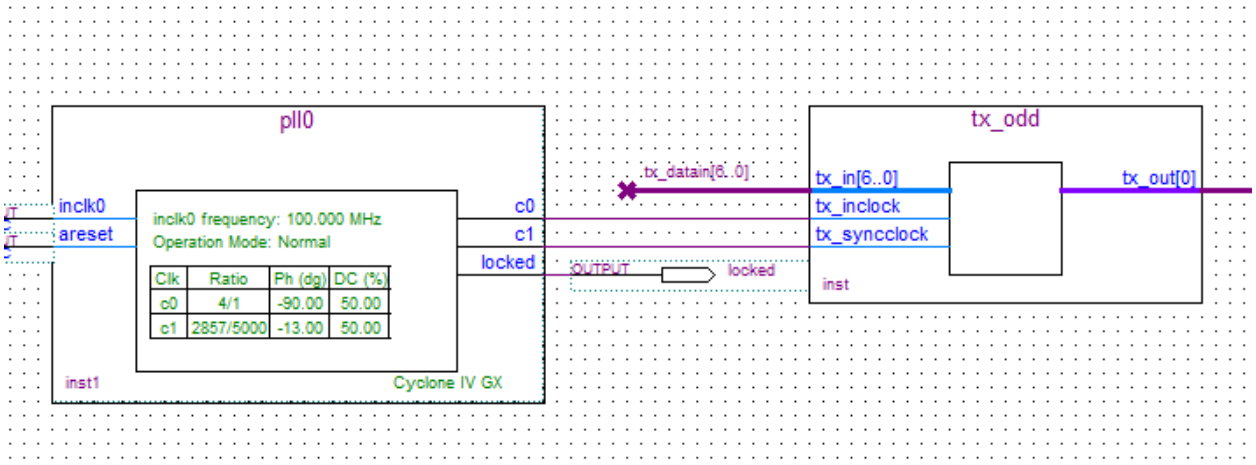

Figure 3-1. Connection between external PLL and ALTLVDS TX with odd serialization factor

The following is a test case to verify the above calculations using internal PLL with soft SERDES in Cyclone IV devices.

Settings:

Data rate = 800Mbps, Serialization factor = 7

PLL Usage

	Name	Output Clock	Mult	Div	Output Frequency	Phase Shift	Phase Shift Step	Duty Cycle
1	altlvds_tx3:inst|altlvds_tx:ALTLVDS_TX_component|altlvds_tx3_lvds_tx:auto_generated|fast_clock	clock0	40	1	400.0 MHz	-90 (-625 ps)	45.00 (312 ps)	50/50
2	altlvds_tx3:inst|altlvds_tx:ALTLVDS_TX_component...3_lvds_tx:auto_generated|wire_lvds_tx_pll_clk[1]	clock1	40	7	57.14 MHz	-13 (-625 ps)	6.43 (312 ps)	50/50

Figure 3-2. Quartus II Fitter report on the frequency, phase shift and duty cycle for each of the clocks when use the internal PLL with LVDS TX soft SERDES in Cyclone IV devices with data rate = 800Mbps and x7 SERDES factor

Data comparison between Fitter report with internal PLL as shown in Figure 3-2 and calculation for external PLL is shown in Table 3-2

PLL output clocks	Fitter report	Soft SERDES
Fast clock – to tx_inclock	Frequency = 400MHz Phase shift = -90 Duty cycle = 50%	Frequency = data rate / 2 = 800/2 = 400 Phase shift = -180/2 = -90 Duty cycle = 50%
Slow clock – to tx_syncclock	Frequency = 57.14MHz Phase shift = -13 Duty cycle = 50%	Frequency = [data rate / SERDES factor] / 2 = 800/(7x2) = 57.14 Phase shift = [-180 / SERDES factor] / 2 = -180/(7x2)= -13 Duty cycle = 50%

Table 3-2. Data comparison for LVDS TX with x7 serialization factor

4. LVDS TX with even serialization factor

For LVDS TX with even serialization factor, Table 4-1 shows the interface clocks needed between the external PLL and the soft SERDES together with their calculations. Figure 4-1 shows an example of connections between the external PLL and the ALTLVDS TX.

Note:

a. The inputs need to be pre-registered in the logic feeding the transmitter with the slow clock.

PLL output clocks	Soft SERDES
Fast clock – to tx_inclock	Frequency = data rate / 2 Phase shift = -180/2 = -90 Duty cycle = 50%
Slow clock – to tx_syncclock	Frequency = data rate / SERDES factor Phase shift = -180 / SERDES factor Duty cycle = 50%

Table 4-1. Calculations for LVDS TX with even serialization factor

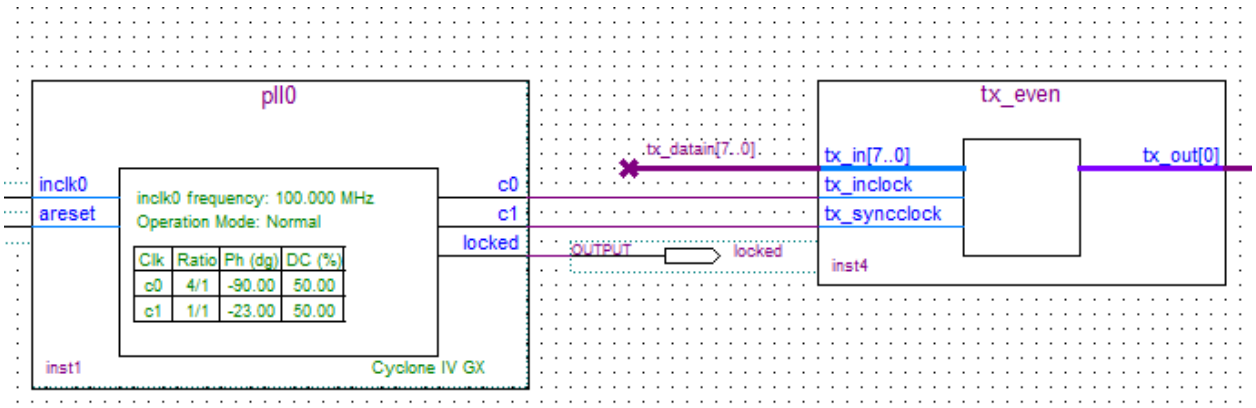

Figure 4-1. Connection between external PLL and ALTLVDS TX with even serialization factor

The following is a test case to verify the above calculations using the internal PLL with soft SERDES in Cyclone IV devices.

Settings:

Data rate = 800Mbps, Serialization factor = 8

PLL Usage

	Name	Output Clock	Mult	Div	Output Frequency	Phase Shift	Phase Shift Step	Duty Cycle
1	altlvds_tx3:inst|altlvds_tx:ALTLVDS_TX_component|altlvds_tx3_lvds_tx:auto_generated|fast_clock	clock0	4	1	400.0 MHz	-90 (-625 ps)	45.00 (312 ps)	50/50
2	altlvds_tx3:inst|altlvds_tx:ALTLVDS_TX_component...3_lvds_tx:auto_generated|wire_lvds_tx_pll_clk[1]	clock1	1	1	100.0 MHz	-23 (-625 ps)	11.25 (312 ps)	50/50

Figure 4-2. Quartus II Fitter report on the frequency, phase shift and duty cycle for each of the clocks when use the internal PLL with LVDS TX soft SERDES in Cyclone IV devices with data rate = 800Mbps and x8 SERDES factor

Data comparison between Fitter report with internal PLL as shown in Figure 4-2 and calculation for external PLL is shown in Table 4-2

PLL output clocks	Fitter report	Soft SERDES
Fast clock – to tx_inclock	Frequency = 400MHz Phase shift = -90 Duty cycle = 50%	Frequency = data rate / 2 = 800/2 = 400 Phase shift = -180/2 = -90 Duty cycle = 50%
Slow clock – to tx_syncclock	Frequency = 100MHz Phase shift = -23 Duty cycle = 50%	Frequency = data rate / SERDES factor = 800/8 = 100 Phase shift = -180 / SERDES factor = -180/8 = -23 Duty cycle = 50%

Table 4-2. Data comparison for LVDS TX with x8 serialization factor

5. LVDS RX with odd serialization factor

For LVDS RX with odd serialization factor, Table 5-1 shows the interface clocks needed between the external PLL and the soft SERDES together with their calculations. Figure 5-1 shows an example of connections between external PLL and the ALTLVDS RX.

Note:

a. The outputs need to be registered in the logic fed by the receiver with the read clock.

PLL output clocks	Soft SERDES
Fast clock – to rx_inclock	Frequency = data rate / 2 Phase shift = -180/2 = -90 Duty cycle = 50%
Slow clock – to rx_syncclock	Frequency = [data rate / SERDES factor] / 2 Phase shift = [-180 / SERDES factor] / 2 Duty cycle = 50%
Read clock – to rx_readclock	Frequency = data rate / SERDES factor Phase shift = -180 / SERDES factor Duty cycle = 50%

Table 5-1. Calculations for LVDS RX with odd deserialization factor

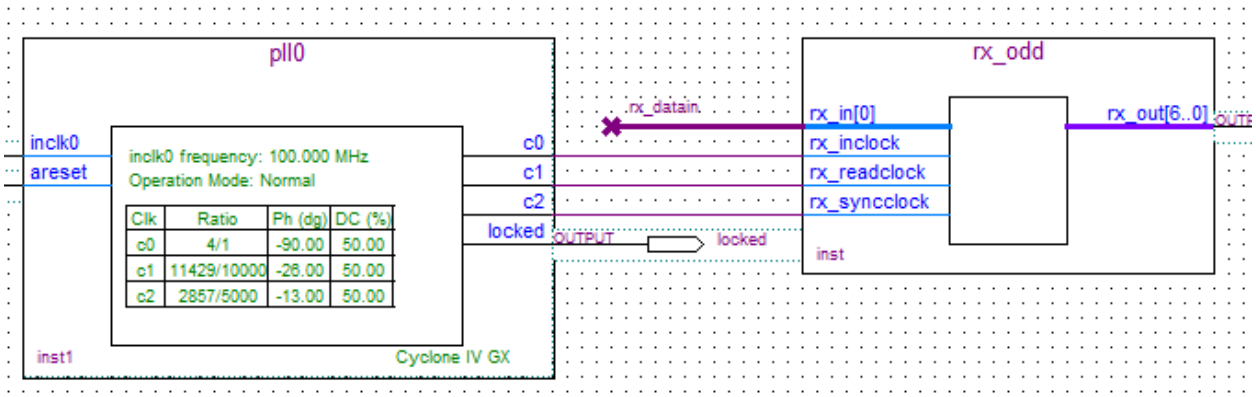

Figure 5-1. Connection between external PLL and ALTLVDS RX with odd deserialization factor

The following is a test case to verify the above calculations using internal PLL with soft SERDES in Cyclone IV devices.

Setting:

Data rate = 800Mbps, Serialization factor = 7

PLL Usage

	Name	Output Clock	Mult	Div	Output Frequency	Phase Shift	Phase Shift Step	Duty Cycle
1	rx_odd:inst|altlvds_rx:ALTLVDS_RX_component|rx_odd_lvds_rx:auto_generated|fast_clock	clock0	4	1	400.0 MHz	-90 (-625 ps)	22.50 (156 ps)	50/50
2	rx_odd:inst|altlvds_rx:ALTLVDS_RX_component|rx_odd_lvds_rx:auto_generated|slow_clock	clock1	4	7	57.14 MHz	-13 (-625 ps)	3.21 (156 ps)	50/50
3	rx_odd:inst|altlvds_rx:ALTLVDS_RX_component|rx_odd_lvds_rx:auto_generated|read_clock	clock2	8	7	114.29 MHz	-26 (-625 ps)	6.43 (156 ps)	50/50

Figure 5-2. Quartus II Fitter report on the frequency, phase shift and duty cycle for each of the clocks when use the internal PLL with LVDS RX soft SERDES in Cyclone IV devices with data rate = 800Mbps and x7 SERDES factor

Data comparison between Fitter report with internal PLL as shown in Figure 5-2 and calculation for external PLL is shown in Table 5-2

PLL output clocks	Fitter report	Soft SERDES
Fast clock – to rx_inclock	Frequency = 400MHz Phase shift = -90 Duty cycle = 50%	Frequency = data rate / 2 = 800/2 = 400 Phase shift = -180/2 = -90 Duty cycle = 50%
Slow clock – to rx_syncclock	Frequency = 57.14MHz Phase shift = -13 Duty cycle = 50%	Frequency = [data rate / SERDES factor] / 2 = 800/(7x2) = 57.14 Phase shift = [-180 / SERDES factor] / 2 = -180/(7x2)= -13 Duty cycle = 50%
Read clock – to rx_readclock	Frequency = 114.29 Phase shift = -26 Duty cycle = 50%	Frequency = data rate / SERDES factor = 800/5 = 114.29 Phase shift = -180 / SERDES factor = -180/7 = -26 Duty cycle = 50%

Table 5-2. Data comparison for LVDS RX with x7 deserialization factor

6. LVDS RX with even serialization factor

For LVDS RX with even serialization factor, Table 6-1 shows the interface clocks needed between the external PLL and the soft SERDES together with their calculations. Figure 6-1 shows an example of connections between the external PLL and the ALTLVDS RX.

Note:

a. The outputs need to be registered in the logic fed by the receiver with the slow clock.

PLL output clocks	Soft SERDES
Fast clock – to rx_inclock	Frequency = data rate / 2 Phase shift = -180/2 = -90 Duty cycle = 50%
Slow clock – to rx_syncclock	Frequency = [data rate / SERDES factor] Phase shift = [-180 / SERDES factor] Duty cycle = 50%

Table 6-1. Calculations for LVDS RX with even deserialization factor

The following is a test case to verify the above calculations using the internal PLL with soft SERDES in Cyclone IV devices.

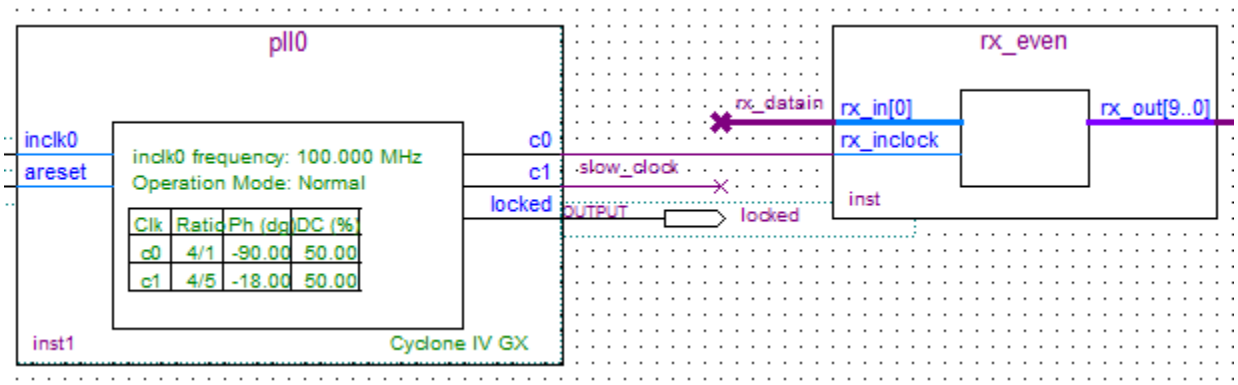

Figure 6-1. Connection between external PLL and ALTLVDS RX with even deserialization factor

Setting:

Data rate = 800Mbps, Serialization factor = 10

PLL Usage

	Name	Output Clock	Mult	Div	Output Frequency	Phase Shift	Phase Shift Step	Duty Cycle
1	altlvds_rx3:inst1|altlvds_rx:ALTLVDS_RX_component|altlvds_rx3_lvds_rx:auto_generated|fast_clock	clock0	4	1	400.0 MHz	-90 (-625 ps)	45.00 (312 ps)	50/50
2	altlvds_rx3:inst1|altlvds_rx:ALTLVDS_RX_componen...3_lvds_rx:auto_generated|wire_lvds_rx_pll_clk[1]	clock1	4	5	80.0 MHz	-18 (-625 ps)	9.00 (312 ps)	50/50

Figure 6-2. Quartus II Fitter report on the frequency, phase shift and duty cycle for each of the clocks when use the internal PLL with LVDS RX soft SERDES in Cyclone IV devices with data rate = 800Mbps and x10 SERDES factor.

Data comparison between Fitter report with internal PLL as shown in Figure 6-2 and calculation for external PLL is shown in Table 6-2

PLL output clocks	Fitter report	Soft SERDES
Fast clock – to rx_inclock	Frequency = 400MHz Phase shift = -90 Duty cycle = 50%	Frequency = data rate / 2 = 800/2 = 400 Phase shift = -180/2 = -90 Duty cycle = 50%
Slow clock – to rx_syncclock	Frequency = 80MHz Phase shift = -18 Duty cycle = 50%	Frequency = [data rate / SERDES factor] = 800/10 = 80 Phase shift = [-180 / SERDES factor] = -180/10 = -18 Duty cycle = 50%

Table 6-2. Data comparison for LVDS RX with x10 deserialization factor

7. Conclusion

This How-To document shows the calculation for the frequency, phase shift and duty cycle for each of the clocks needed for external PLL mode interface with soft SERDES.

8. Revision History

Revision	Changes Made	Date
V1.0	Initial release.	Dec 2011