Serial Digital Interface Demonstration
for Stratix II GX Devices

Introduction

The serial digital interface (SDI) demonstration for the Stratix® II GX video development board uses two instances of the Altera® SDI MegaCore® function. The Stratix II GX video development board is part of the Audio Video Development Kit, Stratix II GX Edition.

For more information on the Stratix II GX video development board, refer to the *Stratix II GX Video Development Board Reference Manual*; for more information on the SDI MegaCore function, refer to your Altera representative.

This application note describes the following two demonstrations and shows how to demonstrate SDIs with the Stratix II GX video demonstration board:

■ Loopback demonstration, which retransmits the received HD-SDI signal to an HD-SDI analyzer
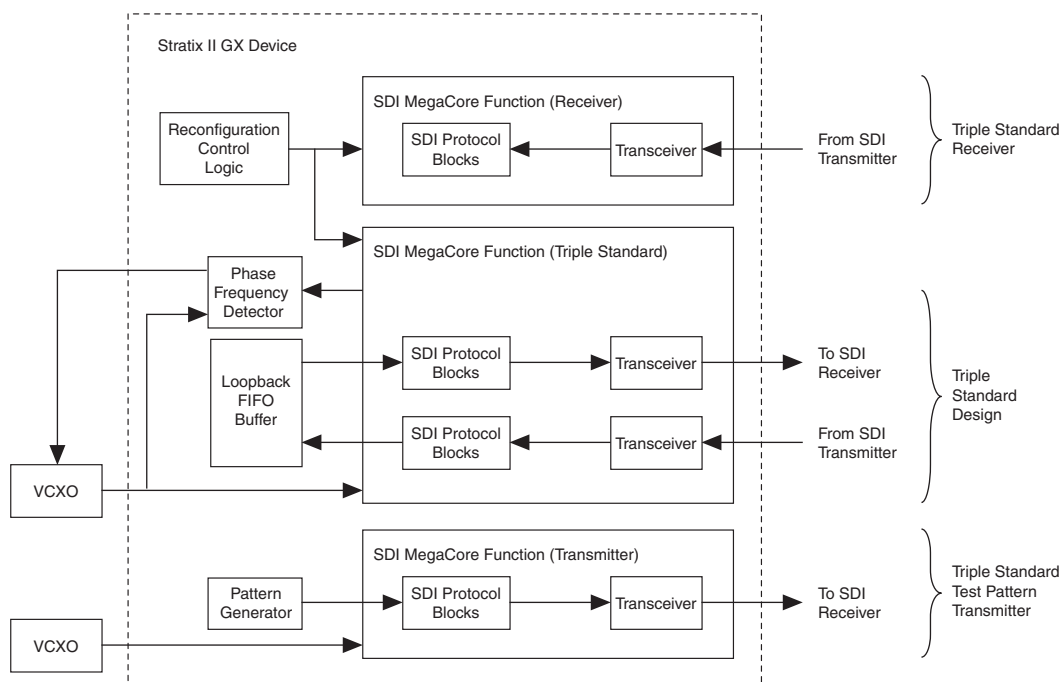■ Test pattern transmitter demonstration

Background

The Stratix II GX family of devices is Altera's third generation of FPGAs to combine high-speed serial transceivers with a scalable, high-performance logic array. Stratix II GX devices include 4 to 20 high-speed transceiver channels, each incorporating clock/data recovery unit (CRU) technology and embedded SERDES capability at data rates of up to 6.375 gigabits per second (Gbps). The transceivers are grouped into four-channel transceiver blocks, and are designed for low power consumption and small die size. The Stratix II GX FPGA technology is built upon the Stratix II architecture, and offers a 1.2-V logic array with unmatched performance, flexibility, and time-to-market capabilities. This scalable, high-performance architecture makes Stratix II GX devices ideal for high-speed backplane interface, chip-to-chip, communications protocol-bridging applications, and various high-speed serial interfaces.

For more information on Stratix II GX devices, refer to the *Stratix II GX Devices Handbook.*

Functional Description

Figure 1 shows the demonstration. The various elements of the demonstration design are described.

Figure 1. Block Diagram

SDI MegaCore Function Triple-Standard Transmitter

The triple-standard SDI transmitter MegaCore function outputs a 2.970-Gbps 1080p, 1.485-Gbps 1080i, or 270-Mbps data stream. It takes its input from the pattern generator.

SDI MegaCore Function Triple-Standard Duplex

The triple standard-SDI duplex MegaCore function provides a full-duplex, 3-Gbps SDI, HD-SDI and SD-SDI and demonstrates receiver-to-transmitter loopback. The received data is decoded, buffered, recoded then transmitted. The interface is configured for 2.970-Gbps, 1.485-Gbps or 270-Mbps rates.

SDI Megacore Function Triple Standard Receiver

The triple-standard SDI receiver MegaCore function provides a 3-Gbps SDI—HD-SDI and SD-SDI receiver interface.

Loopback FIFO Buffer

The decoded receiver data is connected to the transmitter input through a FIFO buffer. When the receiver is locked, the receiver data is written to the FIFO buffer. When the FIFO buffer is half full, the transmitter starts reading, encoding, and transmitting the data.

Phase Frequency Detector

The phase frequency detector takes in the clock data recovery (CDR) clock and the transmitter reference clock and compares their phase and frequency. The phase frequency detector then adjusts the external transmitter reference clock source, so the signals match in phase and frequency. The phase frequency detector allows you to lock a low jitter transmit reference clock to the recovered clock from the SDI input.

Pattern Generator

The pattern generator outputs a 2.970-Gbps 1080p, 1.485-Gbps 1080i or 270-Mbps test pattern. This pattern can be a 100% colorbar, a 75% amplitude colorbar, or an SDI pathological checkfield frame.

Reconfiguration Control Logic

The reconfiguration control logic handles the reconfiguration of the receiver part of the duplex core and the separate receiver in the design. It consists of several subblocks.

Sdi_tr_reconfig_multi
This top-level design contains arbitration logic for up to four receiver ports. This code also has a state machine to control the ALT2GXB_RECONFIG megafunction.

Sdi_4_ch_alt2gxb_reconfig
This block is an ALT2GXB_RECONFIG instance (see the *Stratix II GX Device Handbook*) that is required for DPRIO. Only this megafunction can be used to reprogram the ALT2GXB transceivers.

ROMs
The ROMs hold the ALT2GXB setting information for each of the video standards. Four ROMs are included, which allows up to four channels to be reconfigured.

For more information, refer to the DPRIO section in the *SDI MegaCore Function User Guide*.

Sdi_mif_intercept

This block intercepts the read data from the ROMs. If reprogramming to HD is requested, this block modifies the data out of the ROM before passing it to the ALT2GXB reconfiguration block. The use of this block removes the need to have a ROM for the HD setup.

Getting Started

This section involves the following steps:

- Hardware & Software Requirements
- Install the Design
- Demonstrate an SDI with the Stratix II GX Video Development Board

Hardware & Software Requirements

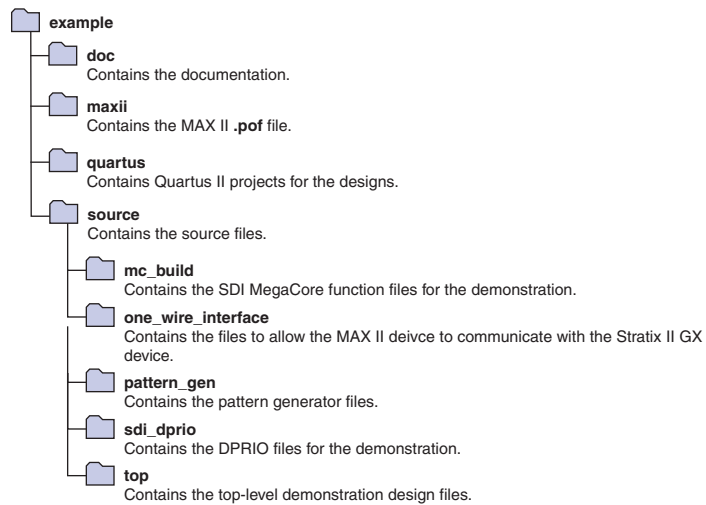The demonstration requires the following hardware:

- Stratix II GX video development board
- SDI MegaCore function
- Quartus® II software, version 7.1

To obtain a Stratix II GX video development board, contact your local Altera representative.

Install the Design

Figure 2 shows the directory structure of the demonstration, which is in the example directory of the SDI MegaCore function.
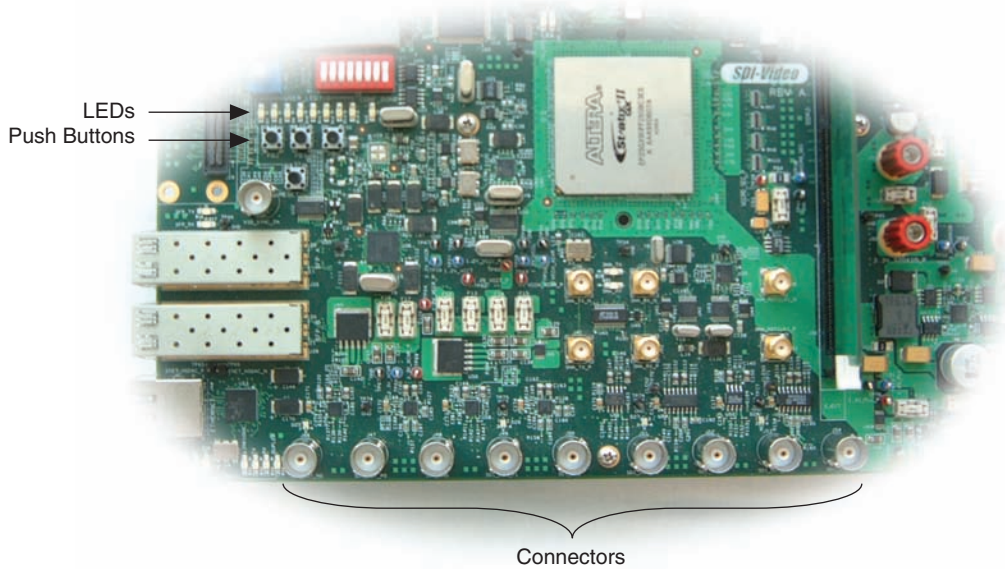
Figure 2. Directory Structure

example

- **doc**
  Contains the documentation.
- **maxii**
  Contains the MAX II **.pof** file.
- **quartus**
  Contains Quartus II projects for the designs.
- **source**
  Contains the source files.
  - **mc_build**
    Contains the SDI MegaCore function files for the demonstration.
  - **one_wire_interface**
    Contains the files to allow the MAX II deivce to communicate with the Stratix II GX device.
  - **pattern_gen**
    Contains the pattern generator files.
  - **sdi_dprio**
    Contains the DPRIO files for the demonstration.
  - **top**
    Contains the top-level demonstration design files.

Demonstrate an SDI with the Stratix II GX Video Development Board

The demonstration shows the functional operation of the SDI, and serial interface performance of the Stratix II GX device on the Stratix II GX video development board.
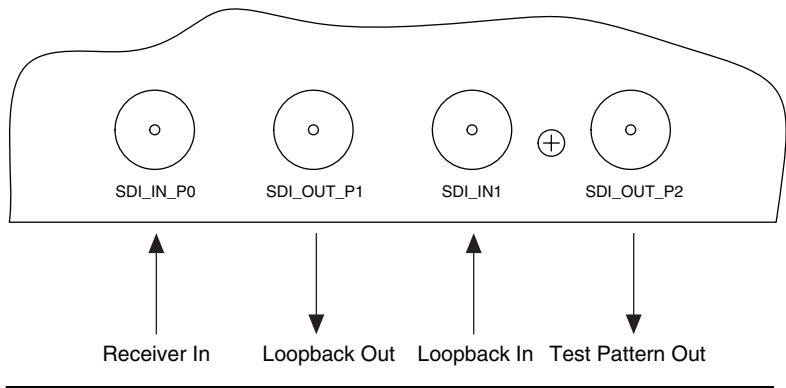
For more information on the Stratix II GX video development board, refer to the *Stratix II GX Video Development Board Reference Manual*.

Figure 3 shows the connectors, LEDs and push buttons on the Stratix II GX Video development board.

Figure 3. Stratix II Video Development Board

To run the demonstration, follow these steps:

1. Setup the board connections:

   a. Connect an SDI signal generator to the receiver input of
      `SDI_IN1` (BNC J51). (see Figure 4).

   b. Connect an SDI signal analyzer to the transmitter output of
      `SDI_OUT_P1` (BNC J50).

   c. Connect the board power supply to the board (J41).

Figure 4. Connections

2. Download the MAX® II file:

   a. Connect the USB-Blaster™ or ByteBlaster™ II download cable to the board socket MAXII (J17).

   b. Power the board and download the **example\maxii\s2gx_sdi_max2_top.pof** file to the MAX II device.

   ☞ This design is stored in nonvolatile memory. If the board is powered down, you do not need to reload this design.

3. Start the Quartus II software.

4. On the File menu click **Open Project**, navigate to **\quartus\tr_sdi.qpf**, and click **Open**.

5. On the Processing menu, click **Start Compilation**.

6. Download the Stratix II GX **.sof** file:

   a. Connect the USB-Blaster™ or ByteBlaster™ II download cable to the board socket labeled SYSTEM JTAG (J24).

   b. Download the Quartus II-generated file **quartus\tr_sdi.sof**.

   ☞ This design is volatile and must be reloaded each time the board is powered on.

7. The loopback demonstration runs. The LEDs indicate the following conditions:

   ● LED3 illuminates when the receiver is word aligned at port 1
   ● LED2 illuminates when the received line format is stable at port 1
   ● LED1 illuminates when the frame format is stable at port 1
   ● LED0 flashes to indicate the presence of the receiver reference clock port 1

   Additionally, the fourth seven-segmet display indicates the following information:

   ● – = unlocked
   ● S = receiver locked to SD-SDI signal
   ● H = receiver locked to HD-SDI signal
   ● 3 = receiver locked to 3-Gbps SDI signal

8. For the test pattern transmitter demonstration, reconnect the SDI signal analyzer to the transmitter output SDI_OUT_P2 (BNC J52). The rotary encoder (SW2) selects either the SD-SDI output, HD-SDI output, or 3-Gbps output. The seven-segment display indicates the following information:

   ● tS = SD-SDI 270-Mbps output
   ● tH = HD-SDI 1.485-Gbps output
   ● t3 = 3-Gbps SDI 2.970-Gbps output

9. The design has a default output of a 75% colorbar pattern. To change this pattern use the PB[0] and PB[1] buttons on the board:

   ● PB[0] selects 100% colorbar output
   ● PB[1] selects a pathological SDI checkfield pattern

10. For the receiver only demonstration, connect an SDI signal generator to the receiver input of SDI_IN_0. The LEDs indicate the following conditions:

   ● LED7 illuminates when the receiver is word aligned port0
   ● LED6 illuminates when the received line format is stable port0
   ● LED5 illuminates when the frame format is stable port0
   ● LED4 flashes to indicate the presence of the receiver referenceclock port 0

Additionally, the third seven-segmet display indicates the following information:

- `−` = unlocked
- `S` = receiver locked to the SD-SDI signal
- `H` = receiver locked to the HD-SDI signal
- `3` = receiver locked to the 3-Gbps SDI signal