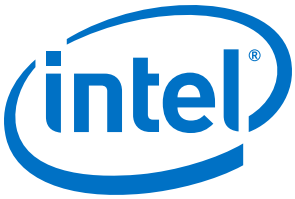

Intel FPGA Download Cable II User Guide

UG-01150 | 2018.04.19
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Contents

1. Setting Up the Intel FPGA Download Cable II

Attention: The download cable has changed name to Intel® FPGA download cable II. Some file names may still refer to USB-Blaster II.

The Intel FPGA download cable II interfaces a USB port on a host computer to an Intel FPGA mounted on a printed circuit board. The download cable sends data from the PC to a standard 10-pin header connected to the FPGA. You can use the cable for the following:

- Iteratively download configuration data to a system during prototyping
- Program data into the system during production
- Advanced Encryption Standard (AES) key and fuse programming

1.1. Supported Devices and Systems

You can use the cable to download configuration data to the following devices:

- Stratix® series FPGAs
- Cyclone® series FPGAs
- MAX® series CPLDs
- Arria® series FPGAs

You can perform in-system programming of the following devices:

- EPC4, EPC8, and EPC16 enhanced configuration devices
- EPCS1, EPCS4, EPCS16, EPCS64, and EPCS/Q128, EPCQ256, EPCQ-L and EPCQ512 serial configuration devices

The cable supports target systems using the following:

- 5.0-V TTL, 3.3-V LVTTL/LVCMOS
- Single-ended I/O standards from 1.5 V to 3.3 V

1.2. Power Source Requirements

- 5.0 V from the cable
- Between 1.5 V and 5.0 V from the target circuit board

1.3. Software Requirements and Support

- Windows 7/8 (32-bit and 64-bit)
- Windows XP (32-bit and 64-bit)
- Windows Server 2008 R2 (64-bit)
- Linux platforms such as Red Hat Enterprise 5

Use the Quartus® Prime software version 14.0 or later to configure your device.

Note: Quartus Prime software version 13.1 supports most of the download cable's capabilities. If you use this version, install the latest patch for full compatibility.

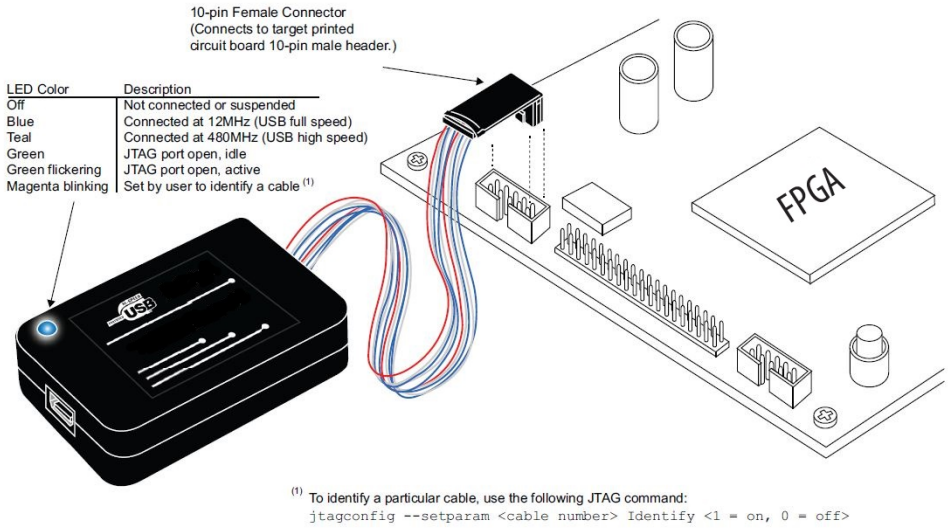
The download cable also supports the following tools:

- Quartus Prime Programmer (and stand-alone version)
- Quartus Prime SignalTap® II Logic Analyzer (and stand-alone version)
- JTAG and debug tools supported by the JTAG Server. For example:
  - System Console
  - Nios II debugger
  - ARM DS-5 debugger

1.4. Installing the Intel FPGA Download Cable II for Configuration or Programming

1. Disconnect the power cable from the circuit board.
2. Connect the cable to the USB port on your computer and to the download cable port.
3. Connect the cable to the 10-pin header on the device board.
4. Reconnect the power cable to reapply power to the circuit board.

Figure 1. The Intel FPGA Download Cable II



Note: For plug and header dimensions, pin names, and operating conditions, see the *Intel FPGA Download Cable II Specifications* chapter.

Related Information

Intel FPGA Download Cable II Specifications on page 8

1.5. Installing the Intel FPGA Download Cable II Driver on Windows 7/8 Systems

You must have system administration (administrator) privileges to install the download cable drivers.

The download cable drivers are included in the Quartus Prime software installation. Before you begin the installation, verify that the download cable driver is located in your directory: \<*Quartus Prime system directory*>**drivers\usb-blaster-ii**.

1. Connect the download cable to your computer's USB port.

   When plugged in for the first time, a message appears stating **Device driver software was not successfully installed**.

2. From the Windows Device Manager, locate **Other devices** and right-click the top **USB-BlasterII**.

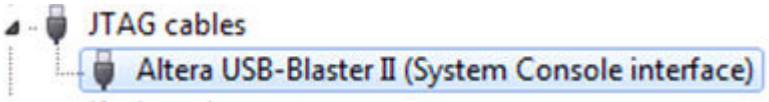
   

   You need to install drivers for each interface: one for the JTAG interface and one for the System Console interface.

3. On the right-click menu, click **Update Driver Software**. The **Update Driver Software - USB BlasterII** dialog appears.

4. Click **Browse my computer for driver software** to continue.
5. Click **Browse...** and browse to the location of the driver on your system: \<*Quartus Prime system directory*>**drivers\usb-blaster-ii**. Click **OK**.
6. Click **Next** to install the driver.
7. Click **Install** when asked if you want to install.

   You should now have a JTAG cable showing in the Device Manager.



8. Now, install the driver for the other interface. Go back to step 2 and repeat the process for the other download cable devices.

   When you are finished, you will have added **USB-Blast II (JTAG interface)** under JTAG cables.

1.6. Installing the Intel FPGA Download Cable II Driver on Linux Systems

For Linux, the download cable supports Red Hat Enterprise 5, 6, and 7.

To access the cable, the Quartus Prime software uses the built-in Red Hat USB drivers, the USB file system (usbfs). By default, **root** is the only user allowed to use usbfs. You must have system administration (root) privileges to configure the Intel FPGA download cable drivers.

1. Create a file named `/etc/udev/rules.d/51-usbblaster.rules` and add the following lines to it. (The **.rules** file may already exist if you have installed an earlier USB-Blaster version.)
   a. Red Hat Enterprise 5 and above

```
# Intel FPGA Download Cable II
SUBSYSTEMS=="usb", ATTRS{idVendor}=="09fb", ATTRS{idProduct}=="6010",
MODE="0666"
SUBSYSTEMS=="usb", ATTRS{idVendor}=="09fb", ATTRS{idProduct}=="6810",
MODE="0666"
```

   Caution: There should be only three lines in this file, one starting with a comment and two starting with BUS. Do not add extra line breaks to the **.rules** file.
2. Complete your installation by setting up the programming hardware in the Quartus Prime software. Go to the "Setting Up the Intel FPGA Download Cable II Hardware with the Quartus Prime Software" section.

For more information about download cable driver installation, refer to the Cable and Adapter Drivers Information page.

Related Information

- Setting Up the Intel FPGA Download Cable II Hardware with the Quartus Prime Software on page 7
- Cable and Adapter Drivers Information

1.7. Installing the Intel FPGA Download Cable II Driver on Windows XP Systems

You must have system administration (administrator) privileges to install the download cable driver.

The download cable drivers are included in the Quartus Prime software installation. Before you begin the installation, verify that the download cable driver is located in your directory: \<*Quartus Prime system directory*>**drivers\usb-blaster-ii**.

1.8. Setting Up the Intel FPGA Download Cable II Hardware with the Quartus Prime Software

1. Start the Quartus Prime software.
2. From the Tools menu, click **Programmer**.
3. Click **Hardware Setup**.
4. Click the **Hardware Settings** tab.
5. From the **Currently selected hardware** list, select **Intel FPGA Download Cable II**.
6. Click **Close**.
7. In the **Mode** list, choose an appropriate programming mode. The table below describes each mode.

Table 1. Programming Modes

Mode	Mode Description
Joint Test Action Group (JTAG)	Programs or configures all devices supported by Quartus Prime software via JTAG programming.
In-Socket Programming	Not supported by the download cable.
Passive Serial Programming	Configures all devices supported by Quartus Prime software excluding enhanced configuration devices (EPC) and serial configuration devices (EPCS/Q).
Active Serial Programming	Programs a single EPCS1, EPCS4, EPCS16, EPCS64, EPCS/Q128, EPCQ256, EPCQ-L and EPCQ512 device.

For detailed help on using the Quartus Prime Programmer, refer to the *Quartus Prime Handbook*.

Related Information

Quartus Prime Handbook

2. Intel FPGA Download Cable II Specifications

2.1. Voltage Requirements

The download cable $V_{CC(TRGT)}$ pin must be connected to a specific voltage for the device being programmed. Connect pull-up resistors to the same power supply as the download cable: $V_{CC(TRGT)}$.

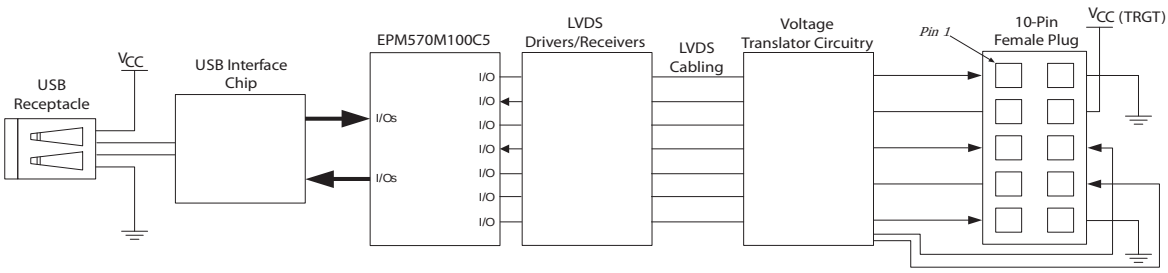
Table 2. Intel FPGA Download Cable II $V_{CC(TRGT)}$ Pin Voltage Requirements

Device Family	Intel FPGA Download Cable II VCC Voltage Required
Arria GX	As specified by V_{CCSEL}
Arria II GX	As specified by V_{CCPD} or V_{CCIO} of Bank 8C
Arria V	As specified by V_{CCPD} Bank 3A
Arria 10	As specified by V_{CCPGM} or V_{CCIO}
Cyclone III	As specified by V_{CCA} or V_{CCIO}
Cyclone IV	As specified by V_{CCIO}. Bank 9 for Cyclone IV GX and Bank 1 for Cyclone IV E devices.
Cyclone V	As specified by V_{CCPD} Bank 3A
EPC4, EPC8, EPC16	3.3 V
EPCS1, EPCS4, EPCS16, EPCS64, EPCS128	3.3 V
EPCS/Q16, EPCS/Q64, EPCS/Q128, EPCQ256, EPCQ512	3.3 V
EPCQ-L	1.8 V
MAX II, MAX V	As specified by V_{CCIO} of Bank 1
MAX 10	As specified by V_{CCIO}
Stratix II, Stratix II GX	As specified by V_{CCSEL}
Stratix III, Stratix IV	As specified by V_{CCPGM} or V_{CCPD}
Stratix V	As specified by V_{CCPD} Bank 3A

2.2. Cable-to-Board Connection

A standard USB cable connects to the USB port on the device.

Figure 2. Intel FPGA Download Cable II Block Diagram



2.3. Intel FPGA Download Cable II Plug Connection

The 10-pin female plug connects to a 10-pin male header on the circuit board containing the target device.

Figure 3. Intel FPGA Download Cable II 10-Pin Female Plug Dimensions - Inches & Millimeters

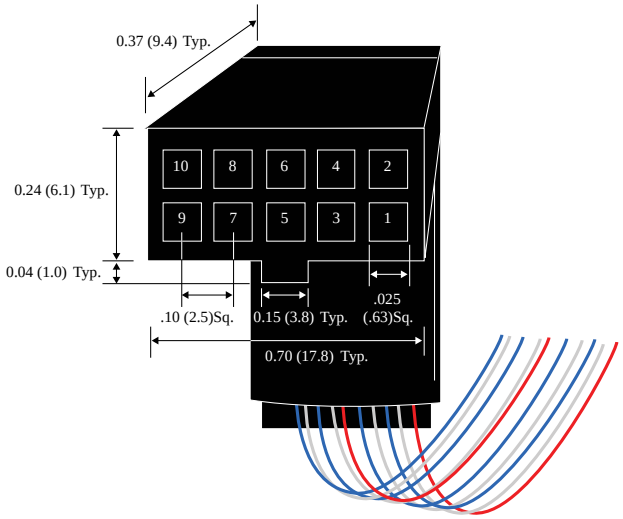
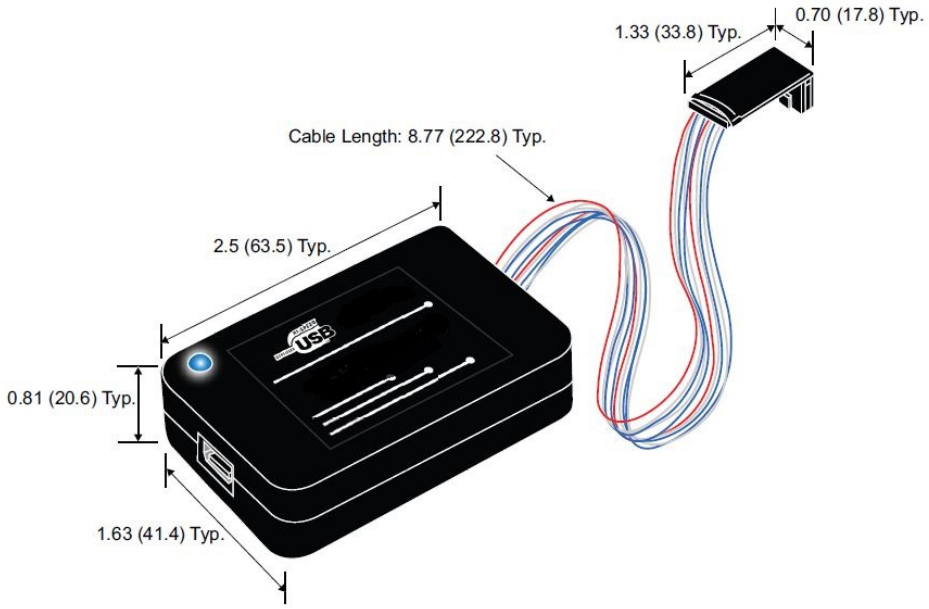


Figure 4. Intel FPGA Download Cable II Dimension - Inches and Millimeters



2.4. 10-Pin Female Plug Signal Names and Programming Modes

Table 3. 10-Pin II Female Plug Signal Names and Programming Modes

Pin	Active Serial (AS) Mode		Passive Serial (PS) Mode		JTAG Mode	
	Signal Name	Description	Signal Name	Description	Signal Name	Description
1	DCLK	Configuration Clock	DCLK	Configuration Clock	TCK	Test Clock
2	GND	Signal ground	GND	Signal ground	GND	Signal ground
3	CONF_DONE	Configuration done	CONF_DONE	Configuration done	TDO	Test Data Output
4	VCC(TRGT)	Target power supply	VCC(TRGT)	Target power supply	VCC(TRGT)	Target power supply
5	nCONFIG	Configuration control	nCONFIG	Configuration control	TMS	Test Mode Select Input
6	nCE	Target chip enable	-	-	PROC_RST	Processor Reset
7	DATAOUT	Active serial data out	nSTATUS	Configuration Status	-	-
8	nCS	Serial configuration device chip select	nCS	Serial configuration device chip select	-	-
9	ASDI	Active serial data in	DATA0	Passive serial data in	TDI	Test Data Input
10	GND	Signal ground	GND	Signal ground	GND	Signal ground

Note: Use pin 6 for hard processor reset under JTAG mode.

Note: The following note below only applies to Intel Arria 10 and earlier SoC devices. PROC_RST is not used for Intel Stratix 10 SoC devices.

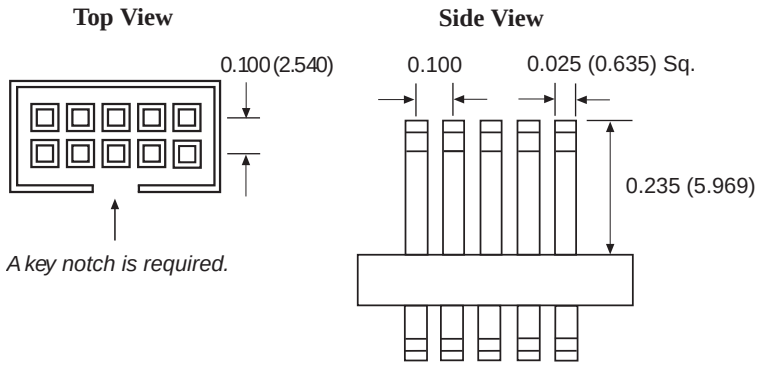
In JTAG mode, the PROC_RST pin can be used to trigger warm reset of the HPS block when prompted via the ARM DS-5 debugger. PROC_RST is an active low signal and not an open collector pin. As such, it is not recommended to connect PROC_RST to HPS_nRST directly. You should instead connect this pin to a secondary device such as the MAX V CPLD, and use the device to manage the reset network for HPS.

2.5. Circuit Board Header Connection

The 10-pin male header, which connects to the download cable's 10-pin female plug, has two rows of five pins. The pins are connected to the device's programming or configuration pins.

Caution: If the header connection on the circuit board is a male receptacle, it must have a key notch. Without a key notch, the 10-pin female plug will not connect. The following figure shows a typical 10-pin male header with a key notch.

Figure 5. 10-Pin Male Header Dimensions - Inches and Millimeters



Although a 10-pin surface mount header can be used for the cable, Intel recommends using a through-hole connector. Through-hole connectors hold up better under the repeated insertion and removal.

2.6. Operating Conditions

The following tables summarize the maximum ratings, recommended operating conditions, and DC operating conditions for the download cable.

Table 4. Intel FPGA Download Cable II Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(TRGT)}$	Target supply voltage	With respect to ground	–0.5	6.5	V
$V_{CC(USB)}$	USB supply voltage	With respect to ground	–0.5	6.0	V

continued...

Symbol	Parameter	Conditions	Min	Max	Unit
I_I	Target side input current	Pin 7	–100.0	100.0	mA
$I_{I(USB)}$	USB supply current	VBUS	–	200.0	mA
I_o	Target side output current	Pins: 1, 5, 6, 8, 9	–50.0	50.0	mA

Table 5. Intel FPGA Download Cable II Recommended Operating Conditions

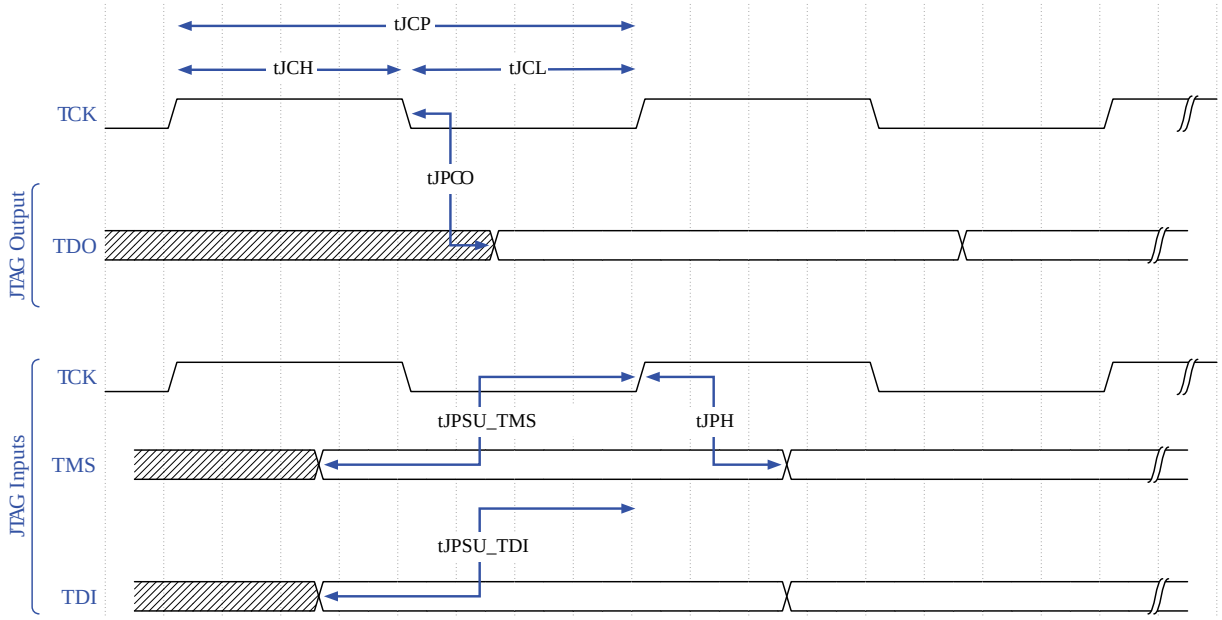
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(TRGT)}$	Target supply voltage, 5.0-V operation	—	4.75	5.25	V
	Target supply voltage, 3.3-V operation	—	3.0	3.6	V
	Target supply voltage, 2.5-V operation	—	2.375	2.625	V
	Target supply voltage, 1.8-V operation	—	1.71	1.89	V
	Target supply voltage, 1.5-V operation	—	1.43	1.57	V

Table 6. Intel FPGA Download Cable II DC Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage	$V_{CC(TRGT)}$ >= 2.0 V	0.7 x $V_{CC(TRGT)}$	—	V
	High-level input voltage	$V_{CC(TRGT)}$ < 2.0 V	0.65 x $V_{CC(TRGT)}$	—	V
V_{IL}	Low-level input voltage	$V_{CC(TRGT)}$ >= 2.0 V	—	0.3 x $V_{CC(TRGT)}$	V
	Low-level input voltage	$V_{CC(TRGT)}$ >= 2.0 V	—	0.2 x $V_{CC(TRGT)}$	V
V_{OH}	5.0-V high-level output voltage	$V_{CC(TRGT)}$ = 4.5 V, I_{OH} = -32 mA	3.8	—	V
	3.3-V high-level output voltage	$V_{CC(TRGT)}$ = 3.0 V, I_{OH} = -24 mA	2.4	—	V
	2.5-V high-level output voltage	$V_{CC(TRGT)}$ = 2.3 V, I_{OH} = -12 mA	1.9	—	V
	1.8-V high-level output voltage	$V_{CC(TRGT)}$ = 1.65 V, I_{OH} = -8 mA	1.2	—	V
	1.5-V high-level output voltage	$V_{CC(TRGT)}$ = 1.4 V, I_{OH} = -6 mA	1.0	—	V
V_{OL}	5.0-V low-level output voltage	$V_{CC(TRGT)}$ = 4.5 V, I_{OL} = 32 mA	—	0.55	V
	3.3-V low-level output voltage	$V_{CC(TRGT)}$ = 3.0 V, I_{OL} = 24 mA	—	0.55	V
	2.5-V low-level output voltage	$V_{CC(TRGT)}$ = 2.3 V, I_{OL} = 12mA	—	0.3	V
	1.8-V low-level output voltage	$V_{CC(TRGT)}$ = 1.65 V, I_{OL} = 8mA	—	0.45	V
	1.5-V low-level output voltage	$V_{CC(TRGT)}$ = 1.4 V, I_{OL} = 6mA	—	0.3	V
$I_{CC(TRGT)}$	Operating current (No Load)	$V_{CC(TRGT)}$=5.5 V	—	316	uA

2.7. JTAG Timing Constraints and Waveforms

Figure 6. Timing Waveform for JTAG Signals (From Target Device Perspective)



To use the download cable at the maximum capability (24 MHz), meet the timing constraints like in the tabe below for the target device.

The timing constraints require that you consider device specifications as well as trace propagation delays. If you do not follow the recommended constraints, you might encounter timing issues at 24 MHz. If the target design cannot meet these constraints, reduce the possibility of timing issues by slowing the TCK frequency. See "Changing the TCK Frequency" section for instructions on running the download cable at a slower speed.

Table 7. JTAG Timing Constraints for the Target Device

Symbol	Parameter	Min	Max	Unit
tJCP	TCK clock period	41.67	—	ns
tJCH	TCK clock high time	20.83	—	ns
tJCL	TCK clock low time	20.83	—	ns
tJPCO	JTAG port clock to JTAG Header output	—	5.46 (2.5 V) 2.66 (1.5 V)	ns

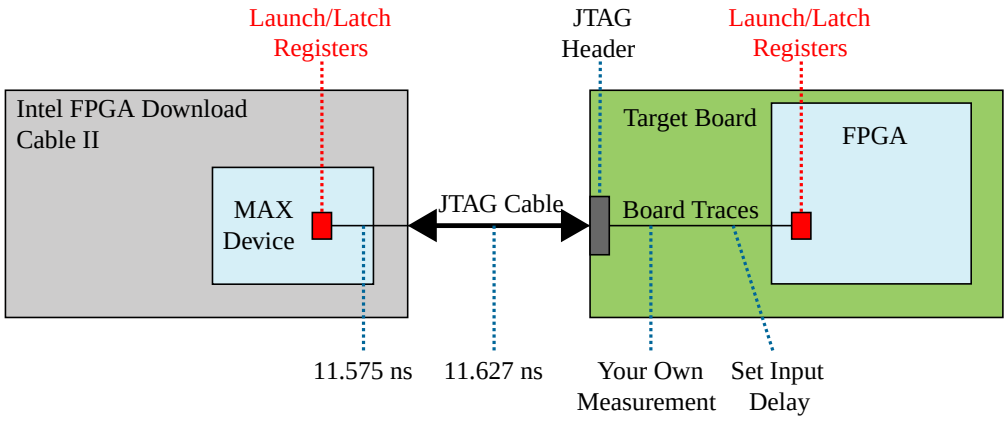
continued...

Symbol	Parameter	Min	Max	Unit
tJPSU_TDI	JTAG port setup time (TDI)	—	24.42	ns
tJPSU_TMS	JTAG port setup time (TMS)	—	26.43	ns
tJPH	JTAG port hold time	—	17.25	ns

The simulated timing is based on a slow timing model, which is a worst-case scenario environment.

For device-specific JTAG timing information, refer to the related device data sheet.

Figure 7. Intel FPGA Download Cable II Timing Constraints



If you cannot meet 24 MHz, you must decrease the frequencies to 16-6 MHz. Below is some example code to set the TCK maximum frequency to 6 MHz:

```
jtagconfig --setparam 1 JtagClock 6M
```

Related Information

- Changing the TCK Frequency on page 14
- Documentation: Data Sheets

2.8. Changing the TCK Frequency

The download cable has a default TCK frequency of 24 MHz. Where signal integrity and timing prevents operating at 24 MHz, change the TCK frequency of the download cable:

1. Open the command line interface with the Intel Quartus Prime `bin` directory in your path (for example, `C:\<Intel Quartus Prime` *`installed folder`*`>\<Intel Quartus Prime` *`version`*`>\quartus\bin64`).
2. Type the following command to change the TCK frequency:

```
jtagconfig --setparam <cable number> JtagClock <frequency><unit prefix>
```

Where:

- <cable number> is the download cable to be modified.
- <frequency> is the desired TCK frequency. Use one the following supported rates:
  - 24 MHz
  - 16 MHz
  - 6 MHz
  - 24/*n* MHz (between 10 kHz and 6 MHz, where *n* represents an integer value number)
- <unit prefix> is the unit prefix for the frequency (e.g., M for MHz).

Example for setting TCK maximum frequency to 6 MHz:

```
jtagconfig --setparam 1 JtagClock 6M
```

A. Additional Information

A.1. Document Revision History

Document Version	Changes
2018.04.19	Updated 10-Pin Female Plug Signal Names and Programming Modes on page 10

Table 8. Intel FPGA Download Cable II User Guide Revision History

Date	Version	Changes
October 2016	2016.10.28	The name USB-Blaster II has changed to Intel FPGA Download Cable II.
December 2015	2015.12.11	Updated Sections: • Supported Devices and Systems • Setting Up the USB-Blaster II Hardware with the Quartus II Software • Voltage Requirements • 10-Pin Female Plug Signal Names and Programming Modes
September 2014	1.2	• Added that the USB-II download cable supports Advanced Encryption Standard (AES) key and fuse programming. • Added magenta LED color to Figure 1-1 supporting multiple cable use. • Clarified a cross reference pointing to device-specific JTAG timing information.
June 2014	1.1	• Added LED color table to Figure 1-1. • Added "JTAG Timing Constraints and Waveforms" section. • Added "Changing the TCK Frequency" section.
January 2014	1.0	Initial release.

A.2. Certification Statements

A.2.1. RoHS Compliance

The table below lists hazardous substances included with the download cable.

A value of 0 indicates that the concentration of the hazardous substance in all homogeneous materials in the parts is below the relevant threshold as specified by the SJ/T11363-2006 standard.

Table 9. Hazardous Substances and Concentration

Part Name	Lead (Pb)	Cadmium (Cd)	Hexavelent Chromium (Cr6+)	Mercury (Hg)	Polybrominated biphenyls (PBB)	Polybrominated diphenyl Ethers (PBDE)
Electronic Components	0	0	0	0	0	0
Populated Circuit Board	0	0	0	0	0	0
Manufacturing Process	0	0	0	0	0	0
Packing	0	0	0	0	0	0

A.2.2. USB 2.0 Certification

This product is USB 2.0 certified.

A.2.3. CE EMI Conformity Caution

This board is delivered conforming to relevant standards mandated by Directive 2004/108/EC. Because of the nature of programmable logic devices, it is possible for the user to modify the kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as the result of modifications to the delivered material is the responsibility of the user.

CE